### III SEMESTER

<table>
<thead>
<tr>
<th>Sl. No</th>
<th>Subject Code</th>
<th>Title</th>
<th>Teaching Dept.</th>
<th>Teaching Hours /Week</th>
<th>Examination</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Theory</td>
<td>Practical/Drawing</td>
</tr>
<tr>
<td>1</td>
<td>10MAT31</td>
<td>Engg. Mathematics - III</td>
<td>Mat</td>
<td>04</td>
<td>03</td>
</tr>
<tr>
<td>2</td>
<td>10ES32</td>
<td>Analog Electronic Ckts</td>
<td>@</td>
<td>04</td>
<td>03</td>
</tr>
<tr>
<td>3</td>
<td>10ES33</td>
<td>Logic Design</td>
<td>@</td>
<td>04</td>
<td>03</td>
</tr>
<tr>
<td>4</td>
<td>10ES34</td>
<td>Network Analysis</td>
<td>@</td>
<td>04</td>
<td>03</td>
</tr>
<tr>
<td>5</td>
<td>10IT35</td>
<td>Electronic Instrumentation</td>
<td>@</td>
<td>04</td>
<td>03</td>
</tr>
<tr>
<td>6</td>
<td>10ES36</td>
<td>Field Theory</td>
<td>@</td>
<td>04</td>
<td>03</td>
</tr>
<tr>
<td>7</td>
<td>10ESL37</td>
<td>Analog Electronics Lab</td>
<td>@</td>
<td>03</td>
<td>03</td>
</tr>
<tr>
<td>8</td>
<td>10ESL38</td>
<td>Logic Design Lab</td>
<td>@</td>
<td>03</td>
<td>03</td>
</tr>
<tr>
<td><strong>TOTAL</strong></td>
<td></td>
<td></td>
<td></td>
<td><strong>24</strong></td>
<td><strong>06</strong></td>
</tr>
</tbody>
</table>

**Note:** @ indicates concerned discipline. ES (for theory) & ECL (for Lab) in the subject code indicates that the subject is common to electrical and electronics stream consisting of EE/EC/IT/TC/ML/BM branches of engineering.
### SCHEME OF TEACHING AND EXAMINATION

**B.E. ELECTRONICS & COMMUNICATION ENGINEERING**  
(Common to EC/TC/ML)

#### IV SEMESTER

<table>
<thead>
<tr>
<th>Sl. No</th>
<th>Subject Code</th>
<th>Title</th>
<th>Dept.</th>
<th>Teaching Hours /Week</th>
<th>Examination</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Theory</td>
<td>Practical/ Drawing</td>
</tr>
<tr>
<td>1</td>
<td>10MAT 41</td>
<td>Engg. Mathematics – IV</td>
<td>Mat</td>
<td>04</td>
<td></td>
</tr>
<tr>
<td>2</td>
<td>10ES 42</td>
<td>Microcontrollers</td>
<td>@</td>
<td>04</td>
<td></td>
</tr>
<tr>
<td>3</td>
<td>10ES43</td>
<td>Control Systems</td>
<td>@</td>
<td>04</td>
<td></td>
</tr>
<tr>
<td>4</td>
<td>10EC 44</td>
<td>Signals &amp; Systems</td>
<td>@</td>
<td>04</td>
<td></td>
</tr>
<tr>
<td>5</td>
<td>10EC45</td>
<td>Fundamentals of HDL</td>
<td>@</td>
<td>04</td>
<td></td>
</tr>
<tr>
<td>6</td>
<td>10EC46</td>
<td>Linear ICs &amp; Applications</td>
<td>@</td>
<td>04</td>
<td></td>
</tr>
<tr>
<td>7</td>
<td>10ESL47</td>
<td>Microcontrollers Lab</td>
<td>@</td>
<td></td>
<td>03</td>
</tr>
<tr>
<td>8</td>
<td>10ECL48</td>
<td>HDL Lab</td>
<td>@</td>
<td></td>
<td>03</td>
</tr>
<tr>
<td><strong>TOTAL</strong></td>
<td></td>
<td></td>
<td></td>
<td><strong>24</strong></td>
<td><strong>06</strong></td>
</tr>
</tbody>
</table>

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<table>
<thead>
<tr>
<th>Sl. No</th>
<th>Subject Code</th>
<th>Title</th>
<th>Teaching Dept.</th>
<th>Teaching Hours /Week</th>
<th>Examination</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Theory</td>
<td>Practical/ Drawing</td>
</tr>
<tr>
<td>1</td>
<td>10AL51</td>
<td>Management and Entrepreneurship</td>
<td>@</td>
<td>4</td>
<td>-</td>
</tr>
<tr>
<td>2</td>
<td>10EC52</td>
<td>Digital Signal Processing</td>
<td>EC</td>
<td>4</td>
<td>-</td>
</tr>
<tr>
<td>3</td>
<td>10EC53</td>
<td>Analog Communication</td>
<td>EC</td>
<td>4</td>
<td>-</td>
</tr>
<tr>
<td>4</td>
<td>10EC54</td>
<td>Microwaves and Radar</td>
<td>EC</td>
<td>4</td>
<td>-</td>
</tr>
<tr>
<td>5</td>
<td>10EC55</td>
<td>Information Theory &amp; Coding</td>
<td>EC</td>
<td>4</td>
<td>-</td>
</tr>
<tr>
<td>6</td>
<td>10EC56</td>
<td>Fundamentals of CMOS VLSI</td>
<td>EC</td>
<td>4</td>
<td>-</td>
</tr>
<tr>
<td>7</td>
<td>10ECL57</td>
<td>DSP Lab</td>
<td>EC</td>
<td>-</td>
<td>3</td>
</tr>
<tr>
<td>8</td>
<td>10ECL58</td>
<td>Analog Communication Lab + LIC Lab</td>
<td>EC</td>
<td>-</td>
<td>3</td>
</tr>
<tr>
<td></td>
<td></td>
<td><strong>TOTAL</strong></td>
<td></td>
<td><strong>24</strong></td>
<td><strong>06</strong></td>
</tr>
</tbody>
</table>

@ - Any Engineering department or department of Business study.
## SCHEME OF TEACHING AND EXAMINATION
### B.E. ELECTRONICS & COMMUNICATION ENGINEERING

### VI SEMESTER

<table>
<thead>
<tr>
<th>Sl. No</th>
<th>Subject Code</th>
<th>Title</th>
<th>Teaching Dept.</th>
<th>Teaching Hours /Week</th>
<th>Examination</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Theory</td>
<td>Practical/Drawing</td>
</tr>
<tr>
<td>1</td>
<td>10EC61</td>
<td>Digital Communication</td>
<td>EC</td>
<td>4</td>
<td>-</td>
</tr>
<tr>
<td>2</td>
<td>10EC62</td>
<td>Microprocessors</td>
<td>EC</td>
<td>4</td>
<td>-</td>
</tr>
<tr>
<td>3</td>
<td>10EC63</td>
<td>Microelectronics Circuits</td>
<td>EC</td>
<td>4</td>
<td>-</td>
</tr>
<tr>
<td>4</td>
<td>10EC64</td>
<td>Antennas and Propagation</td>
<td>EC</td>
<td>4</td>
<td>-</td>
</tr>
<tr>
<td>5</td>
<td>10EC65</td>
<td>Operating Systems</td>
<td>EC</td>
<td>4</td>
<td>-</td>
</tr>
<tr>
<td>6</td>
<td>10EC66x</td>
<td><strong>Elective-I (Group A)</strong></td>
<td>EC</td>
<td>4</td>
<td>-</td>
</tr>
<tr>
<td>7</td>
<td>10ECL67</td>
<td>Advanced Communication Lab</td>
<td>EC</td>
<td>-</td>
<td>3</td>
</tr>
<tr>
<td>8</td>
<td>10ECL68</td>
<td>Microprocessor Lab</td>
<td>EC</td>
<td>-</td>
<td>3</td>
</tr>
<tr>
<td></td>
<td><strong>TOTAL</strong></td>
<td></td>
<td></td>
<td>24</td>
<td>06</td>
</tr>
</tbody>
</table>

### Elective – I (Group A)

<table>
<thead>
<tr>
<th>Subject Code</th>
<th>Title</th>
<th>Teaching Hours /Week</th>
<th>Examination</th>
</tr>
</thead>
<tbody>
<tr>
<td>10EC661</td>
<td>Analog and Mixed Mode VLSI Design</td>
<td></td>
<td></td>
</tr>
<tr>
<td>10EC662</td>
<td>Satellite Communications</td>
<td></td>
<td></td>
</tr>
<tr>
<td>10EC663</td>
<td>Random Process</td>
<td></td>
<td></td>
</tr>
<tr>
<td>10EC664</td>
<td>Low Power VLSI Design</td>
<td></td>
<td></td>
</tr>
<tr>
<td>10EC665</td>
<td>Data Structure Using C++</td>
<td></td>
<td></td>
</tr>
<tr>
<td>10EC666</td>
<td>Digital System Design Using Verilog</td>
<td></td>
<td></td>
</tr>
<tr>
<td>10EC667</td>
<td>Virtual Instrumentation</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>
### SCHEME OF TEACHING AND EXAMINATION

#### B.E. ELECTRONICS & COMMUNICATION ENGINEERING

#### VII SEMESTER

<table>
<thead>
<tr>
<th>Sl. No</th>
<th>Subject Code</th>
<th>Title</th>
<th>Teaching Dept.</th>
<th>Teaching Hours /Week</th>
<th>Examination</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Theory</td>
<td>Practical/Drawing</td>
</tr>
<tr>
<td>1</td>
<td>10EC71</td>
<td>Computer Communication Networks</td>
<td>EC</td>
<td>4</td>
<td>-</td>
</tr>
<tr>
<td>2</td>
<td>10EC72</td>
<td>Optical Fiber Communication</td>
<td>EC</td>
<td>4</td>
<td>-</td>
</tr>
<tr>
<td>3</td>
<td>10EC73</td>
<td>Power Electronics</td>
<td>EC</td>
<td>4</td>
<td>-</td>
</tr>
<tr>
<td>4</td>
<td>10EC74</td>
<td>Embedded System Design</td>
<td>EC</td>
<td>4</td>
<td>-</td>
</tr>
<tr>
<td>5</td>
<td>10EC75x</td>
<td>Elective-II (Group B)</td>
<td>EC</td>
<td>4</td>
<td>-</td>
</tr>
<tr>
<td>6</td>
<td>10EC76x</td>
<td>Elective-III (Group C)</td>
<td>EC</td>
<td>4</td>
<td>-</td>
</tr>
<tr>
<td>7</td>
<td>10ECL77</td>
<td>VLSI Lab</td>
<td>EC</td>
<td>-</td>
<td>3</td>
</tr>
<tr>
<td>8</td>
<td>10ECL78</td>
<td>Power Electronics Lab</td>
<td>EC</td>
<td>-</td>
<td>3</td>
</tr>
<tr>
<td><strong>TOTAL</strong></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

**Elective – II (Group B)**

- 10EC751 DSP Algorithms & Architecture
- 10EC752 Micro and Smart Systems Technology
- 10EC753 Artificial Neural Network
- 10EC754 CAD for VLSI
- 10EC755 Applied Embedded System Design*
- 10EC756 Speech Processing

**Elective – III (Group C)**

- 10EC761 Programming in C++
- 10EC762 Real Time Systems
- 10EC763 Image Processing
- 10EC764 Radio Frequency Integrated Circuits
- 10EC765 Wavelet Transforms
- 10EC766 Modeling and Simulation of Data Networks

**NOTE:** *06EC755 Applied Embedded System Design has a LAB component (syllabus is different and in the Theory Examination, questions from Lab experiments will also be there.*)

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## SCHEME OF TEACHING AND EXAMINATION
### B.E. ELECTRONICS & COMMUNICATION ENGINEERING

### VIII SEMESTER

<table>
<thead>
<tr>
<th>Sl. No</th>
<th>Subject Code</th>
<th>Subject Code</th>
<th>Teaching Dept.</th>
<th>Teaching Hours /Week</th>
<th>Examination</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td>Title</td>
<td></td>
<td>Theory</td>
<td>Practical/ Drawing</td>
</tr>
<tr>
<td>1</td>
<td>10EC81</td>
<td>Wireless Communication EC</td>
<td>4 -</td>
<td>3</td>
<td>25</td>
</tr>
<tr>
<td>2</td>
<td>10EC82</td>
<td>Digital Switching Systems EC</td>
<td>4 -</td>
<td>3</td>
<td>25</td>
</tr>
<tr>
<td>3</td>
<td>10EC83x</td>
<td>Elective-IV (Group D) EC</td>
<td>4 -</td>
<td>3</td>
<td>25</td>
</tr>
<tr>
<td>4</td>
<td>10EC84x</td>
<td>Elective-V (Group E) EC</td>
<td>4 -</td>
<td>3</td>
<td>25</td>
</tr>
<tr>
<td>5</td>
<td>10ECP85</td>
<td>Project Work EC</td>
<td>-</td>
<td>6</td>
<td>3</td>
</tr>
<tr>
<td>6</td>
<td>10ECS86</td>
<td>Seminar EC</td>
<td>-</td>
<td>3</td>
<td>50</td>
</tr>
</tbody>
</table>

**TOTAL** 16 09 15 250 500 750

### Elective – IV (Group D)

- 10EC831 Distributed Systems
- 10EC832 Network Security
- 10EC833 Optical Networks
- 10EC834 High Performance Computing Networks
- 10EC835 Internet Engineering

### Elective – V (Group E)

- 10EE841 Multimedia Communication
- 10EC842 Real Time Operating Systems
- 10EC843 GSM
- 10EC844 Ad-hoc Wireless Networks
- 10EC845 Optical Computing
PART-A

UNIT-1
Fourier series
Convergence and divergence of infinite series of positive terms, definition and illustrative examples*
Periodic functions, Dirichlet’s conditions, Fourier series of periodic functions of period \(2\pi\) and arbitrary period, half range Fourier series. Complex form of Fourier Series. Practical harmonic analysis.

7 Hours

UNIT-2
Fourier Transforms
Infinite Fourier transform, Fourier Sine and Cosine transforms, properties, Inverse transforms

6 Hours

UNIT-3
Application of PDE
Various possible solutions of one dimensional wave and heat equations, two dimensional Laplace’s equation by the method of separation of variables, Solution of all these equations with specified boundary conditions. D’Alembert’s solution of one dimensional wave equation.

6 Hours

UNIT-4
Curve Fitting and Optimisation
Curve fitting by the method of least squares- Fitting of curves of the form
\[ y = ax + b, \quad y = ax^2 + bx + c, \quad y = a e^{bx}, \quad y = ax^b \]
Optimization: Linear programming, mathematical formulation of linear programming problem (LPP), Graphical method and simplex method.

7 Hours

PART-B

UNIT-5
Numerical Methods - 1
Numerical Solution of algebraic and transcendental equations: Regula-falsi method, Newton - Raphson method. Iterative methods of solution of a system
of equations: Gauss-seidel and Relaxation methods. Largest eigen value and the corresponding eigen vector by Rayleigh’s power method.

UNIT-6
Numerical Methods – 2
Finite differences: Forward and backward differences, Newton’s forward and backward interpolation formulae. Divided differences - Newton’s divided difference formula, Lagrange’s interpolation formula and inverse interpolation formula.

Numerical integration: Simpson’s one-third, three-eighth and Weddle’s rules (All formulae/rules without proof)

UNIT-7
Numerical Methods – 3
Numerical solutions of PDE – finite difference approximation to derivatives, Numerical solution of two dimensional Laplace’s equation, one dimensional heat and wave equations

UNIT-8
Difference Equations and Z-Transforms
Difference equations: Basic definition; Z-transforms – definition, standard Z-transforms, damping rule, shifting rule, initial value and final value theorems. Inverse Z-transform. Application of Z-transforms to solve difference equations.

Note: * In the case of illustrative examples, questions are not to be set.

TEXT BOOKS:

REFERENCE BOOKS:
ANALOG ELECTRONIC CIRCUITS
(Common to EC/TC/EE/IT/BM/ML)

Sub Code : 10ES32  IA Marks : 25
Hrs/ Week : 04  Exam Hours : 03
Total Hrs. : 52  Exam Marks : 100

PART – A

UNIT 1: Diode Circuits: Diode Resistance, Diode equivalent circuits, Transition and diffusion capacitance, Reverse recovery time, Load line analysis, Rectifiers, Clippers and clammers. 6 Hours

UNIT 2: Transistor Biasing: Operating point, Fixed bias circuits, Emitter stabilized biased circuits, Voltage divider biased, DC bias with voltage feedback, Miscellaneous bias configurations, Design operations, Transistor switching networks, PNP transistors, Bias stabilization. 6 Hours

UNIT 3: Transistor at Low Frequencies: BJT transistor modeling, CE Fixed bias configuration, Voltage divider bias, Emitter follower, CB configuration, Collector feedback configuration, Analysis of circuits $r_e$ model; analysis of CE configuration using $h$- parameter model; Relationship between $h$- parameter model of CE,CC and CE configuration. 7 Hours

UNIT 4: Transistor Frequency Response: General frequency considerations, low frequency response, Miller effect capacitance, High frequency response, multistage frequency effects. 7 Hours

PART – B

UNIT 5:
(a) General Amplifiers: Cascade connections, Cascode connections, Darlington connections. 3 Hours
(b) Feedback Amplifier: Feedback concept, Feedback connections type, Practical feedback circuits. Design procedures for the feedback amplifiers. 4 Hours
UNIT 6:
**Power Amplifiers**: Definitions and amplifier types, series fed class A amplifier, Transformer coupled Class A amplifiers, Class B amplifier operations, Class B amplifier circuits, Amplifier distortions. Designing of Power amplifiers. **7 Hours**

UNIT 7:
**Oscillators**: Oscillator operation, Phase shift Oscillator, Wienbridge Oscillator, Tuned Oscillator circuits, Crystal Oscillator. (BJT Version Only) Simple design methods of Oscillators. **6 Hours**

UNIT 8:
**FET Amplifiers**: FET small signal model, Biasing of FET, Common drain common gate configurations, MOSFETs, FET amplifier networks. **6 Hours**

TEXT BOOK:

REFERENCE BOOKS:

LOGIC DESIGN
(Common to EC/TC/EE/IT/BM/ML)

<table>
<thead>
<tr>
<th>Sub Code</th>
<th>10ES33</th>
<th>IA Marks</th>
<th>25</th>
</tr>
</thead>
<tbody>
<tr>
<td>Hrs/ Week</td>
<td>04</td>
<td>Exam Hours</td>
<td>03</td>
</tr>
<tr>
<td>Total Hrs.</td>
<td>52</td>
<td>Exam Marks</td>
<td>100</td>
</tr>
</tbody>
</table>

PART – A

UNIT 1:
**Principles of combinational logic-1**: Definition of combinational logic, Canonical forms, Generation of switching equations from truth tables,
Karnaugh maps-3, 4 and 5 variables, Incompletely specified functions (Don’t Care terms), Simplifying Max term equations. 6 Hours

UNIT 2:
Principles of combinational Logic-2: Quine-McCluskey minimization technique- Quine-McCluskey using don’t care terms, Reduced Prime Implicant Tables, Map entered variables. 7 Hours

UNIT 3:
Analysis and design of combinational logic - I: General approach, Decoders-BCD decoders, Encoders. 6 Hours

UNIT 4:
Analysis and design of combinational logic - II: Digital multiplexers- Using multiplexers as Boolean function generators. Adders and subtractors- Cascading full adders, Look ahead carry, Binary comparators. Design methods of building blocks of combinational logics. 7 Hours

PART – B

UNIT 5:

UNIT 6:
Sequential Circuits – 2: Characteristic Equations, Registers, Counters - Binary Ripple Counters, Synchronous Binary counters, Counters based on Shift Registers, Design of a Synchronous counters, Design of a Synchronous Mod-6 Counter using clocked JK Flip-Flops Design of a Synchronous Mod-6 Counter using clocked D, T, or SR Flip-Flops 7 Hours

UNIT 7:
Sequential Design - I: Introduction, Mealy and Moore Models, State Machine Notation, Synchronous Sequential Circuit Analysis and Design. 6 Hours
UNIT 8:
Sequential Design - II: Construction of state Diagrams, Counter Design.  

6 Hours

TEXT BOOKS:

REFERENCE BOOKS:

NETWORK ANALYSIS
(Common to EC/TC/EE/IT/BM/ML)

<table>
<thead>
<tr>
<th>Sub Code</th>
<th>IA Marks</th>
</tr>
</thead>
<tbody>
<tr>
<td>10ES34</td>
<td>25</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Hrs/ Week</th>
<th>Exam Hours</th>
</tr>
</thead>
<tbody>
<tr>
<td>04</td>
<td>03</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Total Hrs.</th>
<th>Exam Marks</th>
</tr>
</thead>
<tbody>
<tr>
<td>52</td>
<td>100</td>
</tr>
</tbody>
</table>

PART – A

UNIT 1:
Basic Concepts: Practical sources, Source transformations, Network reduction using Star – Delta transformation, Loop and node analysis With linearly dependent and independent sources for DC and AC networks, Concepts of super node and super mesh. 7 Hours

UNIT 2:
Network Topology: Graph of a network, Concept of tree and co-tree, incidence matrix, tie-set, tie-set and cut-set schedules, Formulation of equilibrium equations in matrix form, Solution of resistive networks, Principle of duality. 7 Hours

UNIT 3:
Network Theorems – 1: Superposition, Reciprocity and Millman’s theorems. 6 Hours
UNIT 4:
Network Theorems - II:
Thevinin’s and Norton’s theorems; Maximum Power transfer theorem.

6 Hours

PART – B


7 Hours

UNIT 6:
Transient behavior and initial conditions: Behavior of circuit elements under switching condition and their Representation, evaluation of initial and final conditions in RL, RC and RLC circuits for AC and DC excitations.

7 Hours

UNIT 7:

6 Hours

UNIT 8:
Two port network parameters: Definition of z, y, h and transmission parameters, modeling with these parameters, relationship between parameters sets.

6 Hours

TEXT BOOKS:

REFERENCE BOOKS:
ELECTRONIC INSTRUMENTATION
(Common to EC/TC/IT/BM/ML)

Sub Code : 10IT35  IA Marks : 25
Hrs/ Week : 04  Exam Hours : 03
Total Hrs. : 52  Exam Marks : 100

PART – A

UNIT – 1:
Introduction
(a) Measurement Errors: Gross errors and systematic errors, Absolute and relative errors, Accuracy, Precision, Resolution and Significant figures.
(b) Voltmeters and Multimeters: Introduction, Multirange voltmeter, Extending voltmeter ranges, Loading, AC voltmeter using Rectifiers – Half wave and full wave, Peak responding and True RMS voltmeters.

3 + 4 Hours

UNIT – 2:
Digital Instruments

6 Hours

UNIT – 3:
Oscilloscopes
Introduction, Basic principles, CRT features, Block diagram and working of each block, Typical CRT connections, Dual beam and dual trace CROs, Electronic switch.

6 Hours

UNIT – 4:
Special Oscilloscopes
Delayed time-base oscilloscopes, Analog storage, Sampling and Digital storage oscilloscopes.

6 Hours

PART – B

UNIT – 5:
Signal Generators
Introduction, Fixed and variable AF oscillator, Standard signal generator, Laboratory type signal generator, AF sine and Square wave generator,
Function generator, Square and Pulse generator, Sweep frequency generator, Frequency synthesizer. **6 Hours**

UNIT – 6:  
**Measurement of resistance, inductance and capacitance**  
Whetstone’s bridge, Kelvin Bridge; AC bridges, Capacitance Comparison Bridge, Maxwell’s bridge, Wein’s bridge, Wagner’s earth connection. **5 Hours**

UNIT – 7:  
**Transducers - I**  
Introduction, Electrical transducers, Selecting a transducer, Resistive transducer, Resistive position transducer, Strain gauges, Resistance thermometer, Thermistor, Inductive transducer, Differential output transducers and LVDT. **6 Hours**

UNIT – 8:  
**Miscellaneous Topics**  
(a) **Transducers - II** – Piezoelectric transducer, Photoelectric transducer, Photovoltaic transducer, Semiconductor photo devices, Temperature transducers-RTD, Thermocouple.  
(b) **Display devices:** Digital display system, classification of display, Display devices, LEDs, LCD displays.  
(c) Bolometer and RF power measurement using Bolometer  
(d) Introduction to Signal conditioning.  
(e) Introduction to LabView. **10 Hours**

**TEXT BOOKS:**  

**REFERENCE BOOKS:**  
**FIELD THEORY**  
(Common to EC/TC/ML/EE)

<table>
<thead>
<tr>
<th>Sub Code</th>
<th>IA Marks</th>
<th>Hrs/Week</th>
<th>Exam Hours</th>
<th>Total Hrs.</th>
<th>Exam Marks</th>
</tr>
</thead>
<tbody>
<tr>
<td>10ES36</td>
<td>25</td>
<td>04</td>
<td>03</td>
<td>52</td>
<td>100</td>
</tr>
</tbody>
</table>

**PART – A**

**UNIT 1:**

a. **Coulomb’s Law and electric field intensity:** Experimental law of Coulomb, Electric field intensity, Field due to continuous volume charge distribution, Field of a line charge.  

b. **Electric flux density, Gauss’ law and divergence:** Electric flux density, Gauss’ law, Divergence, Maxwell’s First equation(Electrostatics), vector operator $\nabla$ and divergence theorem.

**UNIT 2:**

a. **Energy and potential:** Energy expended in moving a point charge in an electric field, The line integral, Definition of potential difference and Potential, The potential field of a point charge and system of charges, Potential gradient, Energy density in an electrostatic field.

b. **Conductors, dielectrics and capacitance:** Current and current density, Continuity of current, metallic conductors, Conductor properties and boundary conditions, boundary conditions for perfect Dielectrics, capacitance and examples.

**UNIT 3:**

**Poisson’s and Laplace’s equations:** Derivations of Poisson’s and Laplace’s Equations, Uniqueness theorem, Examples of the solutions of Laplace’s and Poisson’s equations.

**UNIT 4:**

**The steady magnetic field:** Biot-Savart law, Ampere’s circuital law, Curl, Stokes’ theorem, magnetic flux and flux density, scalar and Vector magnetic potentials.
PART – B

UNIT 5:
a. Magnetic forces: Force on a moving charge and differential current element, Force between differential current elements, Force and torque on a closed circuit. 4 Hours

b. Magnetic materials and inductance: Magnetization and permeability, Magnetic boundary conditions, Magnetic circuit, Potential energy and forces on magnetic materials, Inductance and Mutual Inductance. 4 Hours

UNIT 6:
Time varying fields and Maxwell’s equations: Faraday’s law, displacement current, Maxwell’s equation in point and Integral form, retarded potentials. 6 Hours

UNIT 7:
Uniform plane wave: Wave propagation in free space and dielectrics, Poynting’s theorem and wave power, propagation in good conductors – (skin effect). 6 Hours

UNIT 8:
Plane waves at boundaries and in dispersive media: Reflection of uniform plane waves at normal incidence, SWR, Plane wave propagation in general directions. 6 Hours

TEXT BOOK:

REFERENCE BOOKS:
ANALOG ELECTRONICS LAB
(Common to EC/TC/EE/IT/BM/ML)

Sub Code : 10ESL37   IA Marks : 25
Hrs/ Week : 03   Exam Hours : 03
Total Hrs. : 42   Exam Marks : 50

NOTE: Use the Discrete components to test the circuits. LabView can be used for the verification and testing along with the above.

1. Wiring of RC coupled Single stage FET & BJT amplifier and determination of the gain-frequency response, input and output impedances.

2. Wiring of BJT Darlington Emitter follower with and without bootstrapping and determination of the gain, input and output impedances (Single circuit) (One Experiment)

3. Wiring of a two stage BJT Voltage series feed back amplifier and determination of the gain, Frequency response, input and output impedances with and without feedback (One Experiment)

4. Wiring and Testing for the performance of BJT-RC Phase shift Oscillator for $f_0 \leq 10$ KHz

5. Testing for the performance of BJT – Hartley & Colpitts Oscillators for RF range $f_0 \geq 100$KHz.

6. Testing for the performance of BJT -Crystal Oscillator for $f_0 > 100$ KHz

7 Testing of Diode clipping (Single/Double ended) circuits for peak clipping, peak detection

8. Testing of Clamping circuits: positive clamping /negative clamping.

9. Testing of a transformer less Class – B push pull power amplifier and determination of its conversion efficiency.

10. Testing of Half wave, Full wave and Bridge Rectifier circuits with and without Capacitor filter. Determination of ripple factor, regulation and efficiency

11. Verification of Thevinin’s Theorem and Maximum Power Transfer theorem for DC Circuits.

LOGIC DESIGN LAB
(Common to EC/TC/EE/IT/BM/ML)

Sub Code : 10ESL38   IA Marks : 25
Hrs/ Week : 03   Exam Hours : 03
Total Hrs. : 42   Exam Marks : 50

NOTE: Use discrete components to test and verify the logic gates. LabView can be used for designing the gates along with the above.

1. Simplification, realization of Boolean expressions using logic gates/Universal gates.
2. Realization of Half/Full adder and Half/Full Subtractors using logic gates.
3. (i) Realization of parallel adder/Subtractors using 7483 chip
   (ii) BCD to Excess-3 code conversion and vice versa.
4. Realization of Binary to Gray code conversion and vice versa
5. MUX/DEMUX – use of 74153, 74139 for arithmetic circuits and code converter.
6. Realization of One/Two bit comparator and study of 7485 magnitude comparator.
7. Use of a) Decoder chip to drive LED display and b) Priority encoder.
8. Truth table verification of Flip-Flops: (i) JK Master slave (ii) T type and (iii) D type.
9. Realization of 3 bit counters as a sequential circuit and MOD – N counter design (7476, 7490, 74192, 74193).
10. Shift left; Shift right, SIPO, SISO, PISO, PIPO operations using 74S95.
11. Wiring and testing Ring counter/Johnson counter.
12. Wiring and testing of Sequence generator.
PART – A

UNIT 1:
Numerical Methods

UNIT 2:
Complex Variables
Function of a complex variable, Limit, Continuity Differentiability – Definitions. Analytic functions, Cauchy – Riemann equations in cartesian and polar forms, Properties of analytic functions. Conformal Transformation – Definition. Discussion of transformations: \( W = z^2 \), \( W = e^z \), \( W = z + \frac{i}{z} \), \( z \neq 0 \) Bilinear transformations.

UNIT 3:
Complex Integration
Complex line integrals, Cauchy’s theorem, Cauchy’s integral formula. Taylor’s and Laurent’s series (Statements only) Singularities, Poles, Residues, Cauchy’s residue theorem (statement only).

UNIT 4:
Series solution of Ordinary Differential Equations and Special Functions

PART – B

UNIT 5:
Statistical Methods
Curve fitting by the method of least squares: \( y = a + bx \), \( y = a + bx + cx^2 \), \( y = ax^b \), \( y = ab^x \), Correlation and Regression.
Probability: Addition rule, Conditional probability, Multiplication rule, Baye’s theorem.

UNIT 6:

UNIT 7:
Sampling, Sampling distribution, Standard error. Testing of hypothesis for means. Confidence limits for means, Student’s t distribution, Chi-square distribution as a test of goodness of fit.

UNIT 8:

TEXT BOOK:
2. Probability by Seymour Lipschutz (Schaum’s series).

REFERENCE BOOKS:
PART – A

UNIT 1:
The 8051 Architecture: Introduction, Architecture of 8051, Pin diagram of 8051, Memory organization, External Memory interfacing, Stacks.

6 Hours

UNIT 2:
Addressing Modes: Introduction, Instruction syntax, Data types, Subroutines, Addressing modes: Immediate addressing, Register addressing, Direct addressing, Indirect addressing, relative addressing, Absolute addressing, Long addressing, Indexed addressing, Bit inherent addressing, bit direct addressing.
Instruction set: Instruction timings, 8051 instructions: Data transfer instructions, Arithmetic instructions, Logical instructions, Branch instructions, Subroutine instructions, Bit manipulation instruction.

6 Hours

UNIT 3:
8051 programming: Assembler directives, Assembly language programs and Time delay calculations.

6 Hours

UNIT 4:
8051 Interfacing and Applications: Basics of I/O concepts, I/O Port Operation, Interfacing 8051 to LCD, Keyboard, parallel and serial ADC, DAC, Stepper motor interfacing and DC motor interfacing and programming

7 Hours

PART – B

UNIT 5:
8051 Interrupts and Timers/counters: Basics of interrupts, 8051 interrupt structure, Timers and Counters, 8051 timers/counters, programming 8051 timers in assembly and C.

6 Hours
UNIT 6:
8051 Serial Communication: Data communication, Basics of Serial Data Communication, 8051 Serial Communication, connections to RS-232, Serial communication Programming in assembly and C.
8255A Programmable Peripheral Interface; Architecture of 8255A, I/O addressing, I/O devices interfacing with 8051 using 8255A.

6 Hours

Course Aim – The MSP430 microcontroller is ideally suited for development of low-power embedded systems that must run on batteries for many years. There are also applications where MSP430 microcontroller must operate on energy harvested from the environment. This is possible due to the ultra-low power operation of MSP430 and the fact that it provides a complete system solution including a RISC CPU, flash memory, on-chip data converters and on-chip peripherals.

UNIT 7:
Motivation for MSP430 microcontrollers – Low Power embedded systems, On-chip peripherals (analog and digital), low-power RF capabilities. Target applications (Single-chip, low cost, low power, high performance system design).

2 Hours

MSP430 RISC CPU architecture, Compiler-friendly features, Instruction set, Clock system, Memory subsystem. Key differentiating factors between different MSP430 families.

2 Hours


3 Hours

Digital I/O – I/O ports programming using C and assembly, Understanding the muxing scheme of the MSP430 pins.

2 Hours

UNIT 8:
On-chip peripherals. Watchdog Timer, Comparator, Op-Amp, Basic Timer, Real Time Clock (RTC), ADC, DAC, SD16, LCD, DMA.

2 Hours

Using the Low-power features of MSP430. Clock system, low-power modes, Clock request feature, Low-power programming and Interrupt.

2 Hours

2 Hours

Case Studies of applications of MSP430 - Data acquisition system, Wired Sensor network, Wireless sensor network with Chipcon RF interfaces.

3 Hours

TEXT BOOKS:

(Indian edition available)

REFERENCE BOOKS:
3. MSP430 Teaching CD-ROM, Texas Instruments, 2008 (can be requested http://www.uniti.in )

CONTROL SYSTEMS
(Common to EC/TC/EE/IT/BM/ML)

Sub Code : 10ES43 IA Marks : 25
Hrs/ Week : 04 Exam Hours : 03
Total Hrs. : 52 Exam Marks : 100

PART – A

UNIT 1:
Modeling of Systems: Introduction to Control Systems, Types of Control Systems, Effect of Feedback Systems, Differential equation of Physical Systems - Mechanical systems, Friction, Translational systems (Mechanical accelerometer, systems excluded), Rotational systems, Gear trains, Electrical systems, Analogous systems. 7 Hours

UNIT 2:
Block diagrams and signal flow graphs: Transfer functions, Block diagram algebra, Signal Flow graphs (State variable formulation excluded), 6 Hours
UNIT 3:
Time Response of feed back control systems: Standard test signals, Unit step response of First and second order systems, Time response specifications, Time response specifications of second order systems, steady – state errors and error constants. Introduction to PID Controllers(excluding design) 7 Hours

UNIT 4:
Stability analysis: Concepts of stability, Necessary conditions for Stability, Routh- stability criterion, Relative stability analysis; More on the Routh stability criterion. 6 Hours

PART – B

UNIT 5:
Root–Locus Techniques: Introduction, The root locus concepts, Construction of root loci. 6 Hours

UNIT 6:
Frequency domain analysis: Correlation between time and frequency response, Bode plots, Experimental determination of transfer functions, Assessment of relative stability using Bode Plots. Introduction to lead, lag and lead-lag compensating networks (excluding design). 7 Hours

UNIT 7:

UNIT 8:
Introduction to State variable analysis: Concepts of state, state variable and state models for electrical systems, Solution of state equations. 6 Hours

TEXT BOOK:

REFERENCE BOOKS:
SIGNALS & SYSTEMS  
(Common to EC/TC/IT/BM/ML)

<table>
<thead>
<tr>
<th>Sub Code</th>
<th>IA Marks</th>
</tr>
</thead>
<tbody>
<tr>
<td>10EC44</td>
<td>25</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Hrs/ Week</th>
<th>Exam Hours</th>
<th>Exam Marks</th>
</tr>
</thead>
<tbody>
<tr>
<td>04</td>
<td>03</td>
<td>100</td>
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Total Hrs.: 52

PART – A

UNIT 1:  
**Introduction**: Definitions of a signal and a system, classification of signals, basic Operations on signals, elementary signals, Systems viewed as Interconnections of operations, properties of systems.  
**6 Hours**

UNIT 2:  
**Time-domain representations for LTI systems – 1**: Convolution, impulse response representation, Convolution Sum and Convolution Integral.  
**6 Hours**

UNIT 3:  
**Time-domain representations for LTI systems – 2**: Properties of impulse response representation, Differential and difference equation Representations, Block diagram representations.  
**7 Hours**

UNIT 4:  
**Fourier representation for signals – 1**: Introduction, Discrete time and continuous time Fourier series (derivation of series excluded) and their properties.  
**7 Hours**

PART – B

UNIT 5:  
**Fourier representation for signals – 2**: Discrete and continuous Fourier transforms (derivations of transforms are excluded) and their properties.  
**6 Hours**

UNIT 6:  
**Applications of Fourier representations**: Introduction, Frequency response of LTI systems, Fourier transform representation of periodic signals, Fourier
transform representation of discrete time signals. Sampling theorem and Nyquist rate.

UNIT 7:

UNIT 8:

TEXT BOOK

REFERENCE BOOKS:

FUNDAMENTALS OF HDL
(Common to EC/TC/IT/BM/ML)

Sub Code : 10EC45 IA Marks : 25
Hrs/ Week : 04 Exam Hours : 03
Total Hrs. : 52 Exam Marks : 100

PART – A

UNIT 1:
Introduction: Why HDL? , A Brief History of HDL, Structure of HDL Module, Operators, Data types, Types of Descriptions, simulation and synthesis, Brief comparison of VHDL and Verilog

7 Hours
UNIT 2:  
Data Flow Descriptions: Highlights of Data-Flow Descriptions, Structure of Data-Flow Description, Data Type – Vectors.  
6 Hours

UNIT 3:  
Behavioral Descriptions: Behavioral Description highlights, structure of HDL behavioral Description, The VHDL variable – Assignment Statement, sequential statements.  
6 Hours

UNIT 4:  
Structural Descriptions: Highlights of structural Description, Organization of the structural Descriptions, Binding, state Machines, Generate, Generic, and Parameter statements.  
7 Hours

PART – B

UNIT 5:  
Procedures, Tasks, and Functions: Highlights of Procedures, tasks, and Functions, Procedures and tasks, Functions.  
Advanced HDL Descriptions: File Processing, Examples of File Processing  
7 Hours

UNIT 6:  
Mixed –Type Descriptions: Why Mixed-Type Description? VHDL User-Defined Types, VHDL Packages, Mixed-Type Description examples  
6 Hours

UNIT 7:  
Mixed –Language Descriptions: Highlights of Mixed-Language Description, How to invoke One language from the Other, Mixed-language Description Examples, Limitations of Mixed-Language Description.  
7 Hours

UNIT 8:  
6 Hours

TEXT BOOKS:  

REFERENCE BOOKS:  
2. VHDL -Douglas perry-Tata McGraw-Hill.  
3. A Verilog HDL Primer- J.Bhaskar – BS Publications  
LINEAR IC’s & APPLICATIONS
(Common to EC/TC/IT/BM/ML)

Sub Code : 10EC46 IA Marks  : 25
Hrs/ Week  : 04 Exam Hours  : 03
Total Hrs. : 52 Exam Marks : 100

PART – A

UNIT 1:
Operational Amplifier Fundamentals: Basic Op-Amp circuit, Op-Amp parameters – Input and output voltage, CMRR and PSRR, offset voltages and currents, Input and output impedances, Slew rate and Frequency limitations; Op-Amps as DC Amplifiers- Biasing Op-Amps, Direct coupled -Voltage Followers, Non-inverting Amplifiers, Inverting amplifiers, Summing amplifiers, Difference amplifier. 7 Hours

UNIT 2:
Op-Amps as AC Amplifiers: Capacitor coupled Voltage Follower, High input impedance - Capacitor coupled Voltage Follower, Capacitor coupled Non-inverting Amplifiers, High input impedance - Capacitor coupled Non-inverting Amplifiers, Capacitor coupled Inverting amplifiers, setting the upper cut-off frequency, Capacitor coupled Difference amplifier, Use of a single polarity power supply. 7 Hours

UNIT 3:
Op-Amps frequency response and compensation: Circuit stability, Frequency and phase response, Frequency compensating methods, Band width, Slew rate effects, $Z_{in}$ Mod compensation, and circuit stability precautions. 6 Hours

UNIT 4:
OP-AMP Applications: Voltage sources, current sources and current sinks, Current amplifiers, instrumentation amplifier, precision rectifiers, Limiting circuits. 6 Hours

PART – B

UNIT 5:
More applications: Clamping circuits, Peak detectors, sample and hold circuits, V to I and I to V converters, Log and antilog amplifiers, Multiplier
and divider, Triangular / rectangular wave generators, Wave form generator design, phase shift oscillator, Wein bridge oscillator. 

UNIT 6:
Non-linear circuit applications: crossing detectors, inverting Schmitt trigger circuits, Monostable & Astable multivibrator, Active Filters – First and second order Low pass & High pass filters. 

UNIT 7:

UNIT 8:
Other Linear IC applications: 555 timer - Basic timer circuit, 555 timer used as astable and monostable multivibrator, Schmitt trigger; PLL-operating principles, Phase detector / comparator, VCO; D/A and A/ D converters – Basic DAC Techniques, AD converters. 

TEXT BOOKS:

REFERENCE BOOKS:
I. PROGRAMMING

3. Counters.
4. Boolean & Logical Instructions (Bit manipulations).
5. Conditional CALL & RETURN.
7. Programs to generate delay, Programs using serial port and on-Chip timer / counter.

Note: Programming exercise is to be done on both 8051 & MSP430.

II. INTERFACING:

Write C programs to interface 8051 chip to Interfacing modules to develop single chip solutions.
8. Simple Calculator using 6 digit seven segment displays and Hex Keyboard interface to 8051.
9. Alphanumeric LCD panel and Hex keypad input interface to 8051.
10. External ADC and Temperature control interface to 8051.
11. Generate different waveforms Sine, Square, Triangular, Ramp etc. using DAC interface to 8051; change the frequency and amplitude.
12. Stepper and DC motor control interface to 8051.
13. Elevator interface to 8051.
HDL LAB
(Common to EC/TC/IT/BM/ML)

Sub Code : 10ECL48  IA Marks : 25
Hrs/ Week : 03  Exam Hours : 03
Total Hrs. : 42  Exam Marks : 50

Note: Programming can be done using any compiler. Download the programs on a FPGA/CPLD boards such as Apex/Acex/Max/Spartan/Sinfi/TK Base or equivalent and performance testing may be done using 32 channel pattern generator and logic analyzer apart from verification by simulation with tools such as Altera/Modelsim or equivalent.

PROGRAMMING (using VHDL /Verilog)

1. Write HDL code to realize all the logic gates
2. Write a HDL program for the following combinational designs
   a. 2 to 4 decoder
   b. 8 to 3 (encoder without priority & with priority)
   c. 8 to 1 multiplexer
   d. 4 bit binary to gray converter
   e. Multiplexer, de-multiplexer, comparator.
3. Write a HDL code to describe the functions of a Full Adder Using three modeling styles.

32

• ALU should use combinational logic to calculate an output based on the four bit op-code input.
• ALU should pass the result to the out bus when enable line in high, and tri-state the out bus when the enable line is low.
• ALU should decode the 4 bit op-code according to the given in example below.
<table>
<thead>
<tr>
<th>OPCODE</th>
<th>ALU OPERATION</th>
</tr>
</thead>
<tbody>
<tr>
<td>1.</td>
<td>A + B</td>
</tr>
<tr>
<td>2.</td>
<td>A – B</td>
</tr>
<tr>
<td>3.</td>
<td>A Complement</td>
</tr>
<tr>
<td>4.</td>
<td>A * B</td>
</tr>
<tr>
<td>5.</td>
<td>A AND B</td>
</tr>
<tr>
<td>6.</td>
<td>A OR B</td>
</tr>
<tr>
<td>7.</td>
<td>A NAND B</td>
</tr>
<tr>
<td>8.</td>
<td>A XOR B</td>
</tr>
</tbody>
</table>

4. Develop the HDL code for the following flip-flops, SR, D, JK, T.
5. Design 4 bit binary, BCD counters (Synchronous reset and Asynchronous reset) and “any sequence” counters

**INTERFACING** (at least four of the following must be covered using VHDL/Verilog)

1. Write HDL code to display messages on the given seven segment display and LCD and accepting Hex key pad input data.
2. Write HDL code to control speed, direction of DC and Stepper motor.
3. Write HDL code to accept 8 channel Analog signal, Temperature sensors and display the data on LCD panel or Seven segment display.
4. Write HDL code to generate different waveforms (Sine, Square, Triangle, Ramp etc.,) using DAC change the frequency and amplitude.
5. Write HDL code to simulate Elevator operations
6. Write HDL code to control external lights using relays.
V SEMESTER
MANAGEMENT & ENTREPRENEURSHIP

Subject Code : 10AL51
IA Marks : 25
No. of Lecture Hrs/Week : 04
Exam Hours : 03
Total no. of Lecture Hrs. : 52
Exam Marks : 100

MANAGEMENT (PART – A )

UNIT - 1
7 Hours

UNIT - 2
PLANNING: Nature, importance and purpose of planning process - Objectives - Types of plans (Meaning only) - Decision making - Importance of planning - steps in planning & planning premises - Hierarchy of plans.
6 Hours

UNIT - 3
7 Hours

UNIT - 4
DIRECTING & CONTROLLING: Meaning and nature of directing - Leadership styles, Motivation Theories, Communication - Meaning and importance – Coordination, meaning and importance and Techniques of Coordination. Meaning and steps in controlling - Essentials of a sound control system - Methods of establishing control.
6 Hours

ENTREPRENEURSHIP (PART – B )

UNIT - 5
ENTREPRENEUR: Meaning of Entrepreneur; Evolution of the Concept, Functions of an Entrepreneur, Types of Entrepreneur, Intrapreneur - an emerging Class. Concept of Entrepreneurship - Evolution of Entrepreneurship, Development of Entrepreneurship; Stages in entrepreneurial process; Role of entrepreneurs in Economic Development; Entrepreneurship in India; Entrepreneurship – its Barriers.
6 Hours
UNIT - 6
SMALL SCALE INDUSTRY: Definition; Characteristics; Need and rationale: Objectives; Scope; role of SSI in Economic Development. Advantages of SSI Steps to start an SSI - Government policy towards SSI; Different Policies of S.S.I.; Government Support for S.S.I. during 5 year plans, Impact of Liberalization, Privatization, Globalization on S.S.I., Effect of WTO/GATT Supporting Agencies of Government for S.S.I Meaning; Nature of Support; Objectives; Functions; Types of Help; Ancillary Industry and Tiny Industry (Definition only).

UNIT - 7
INSTITUTIONAL SUPPORT: Different Schemes; TECKSOK; KIADB; KSSIDC; KSIMC; DIC Single Window Agency; SISI; NSIC; SIDBI; KSFC.

UNIT - 8
PREPARATION OF PROJECT: Meaning of Project; Project Identification; Project Selection; Project Report; Need and Significance of Report; Contents; formulation; Guidelines by Planning Commission for Project report; Network Analysis; Errors of Project Report; Project Appraisal. Identification of Business Opportunities - Market Feasibility Study; Technical Feasibility Study; Financial Feasibility Study & Social Feasibility Study.

TEXT BOOKS:

REFERENCE BOOKS:
2. Entrepreneurship Development - S S Khanka - S Chand & Co.
PART – A

UNIT - 1
Discrete Fourier Transforms (DFT): Frequency domain sampling and reconstruction of discrete time signals. DFT as a linear transformation, its relationship with other transforms.  

UNIT - 2
Properties of DFT, multiplication of two DFTs- the circular convolution, additional DFT properties.  

UNIT - 3
Use of DFT in linear filtering, overlap-save and overlap-add method. Direct computation of DFT, need for efficient computation of the DFT (FFT algorithms).  

UNIT - 4

PART – B

UNIT - 5
IIR filter design: Characteristics of commonly used analog filters – Butterworth and Chebysheve filters, analog to analog frequency transformations.  

UNIT - 6
Implementation of discrete-time systems: Structures for IIR and FIR systems- direct form I and direct form II systems, cascade, lattice and parallel realization.  

UNIT - 7
FIR filter design: Introduction to FIR filters, design of FIR filters using - Rectangular, Hamming, Bartlet and Kaiser windows, FIR filter design using frequency sampling technique.  

36
UNIT - 8
Design of IIR filters from analog filters (Butterworth and Chebyshev) - impulse invariance method. Mapping of transfer functions: Approximation of derivative (backward difference and bilinear transformation) method, Matched z transforms, Verification for stability and linearity during mapping

7 Hours

TEXT BOOK:

REFERENCE BOOKS:

ANALOG COMMUNICATION

<table>
<thead>
<tr>
<th>Subject Code</th>
<th>10EC53</th>
<th>IA Marks</th>
<th>25</th>
</tr>
</thead>
<tbody>
<tr>
<td>No. of Lecture Hrs/Week</td>
<td>04</td>
<td>Exam Hours</td>
<td>03</td>
</tr>
<tr>
<td>Total no. of Lecture Hrs.</td>
<td>52</td>
<td>Exam Marks</td>
<td>100</td>
</tr>
</tbody>
</table>

PART – A

UNIT - 1

7 Hours

UNIT - 2

7 Hours
UNIT - 3
6 Hours

UNIT - 4
6 Hours

PART – B

UNIT - 5
ANGLE MODULATION (FM)-I: Basic definitions, FM, narrow band FM, wide band FM, transmission bandwidth of FM waves, generation of FM waves: indirect FM and direct FM.  
6 Hours

UNIT - 6
ANGLE MODULATION (FM)-II: Demodulation of FM waves, FM stereo multiplexing, Phase-locked loop, Nonlinear model of the phase – locked loop, Linear model of the phase – locked loop, Nonlinear effects in FM systems.  
7 Hours

UNIT - 7
NOISE: Introduction, shot noise, thermal noise, white noise, Noise equivalent bandwidth, Narrow bandwidth, Noise Figure, Equivalent noise temperature, cascade connection of two-port networks.  
6 Hours

UNIT - 8
NOISE IN CONTINUOUS WAVE MODULATION SYSTEMS: Introduction, Receiver model, Noise in DSB-SC receivers, Noise in SSB receivers, Noise in AM receivers, Threshold effect, Noise in FM receivers, FM threshold effect, Pre-emphasis and De-emphasis in FM.  
7 Hours
TEXT BOOKS:
2. An Introduction to Analog and Digital Communication, Simon Haykins, John Wiley India Pvt. Ltd., 2008

REFERENCE BOOKS:
1. Modern digital and analog Communication systems B. P. Lathi, Oxford University Press, 4th ed, 2010,

MICROWAVES AND RADAR

<table>
<thead>
<tr>
<th>Subject Code</th>
<th>IA Marks</th>
</tr>
</thead>
<tbody>
<tr>
<td>10EC54</td>
<td>25</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>No. of Lecture Hrs/Week</th>
<th>Exam Hours</th>
</tr>
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</tr>
</tbody>
</table>

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</tr>
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<td>100</td>
</tr>
</tbody>
</table>

PART – A

UNIT - 1
MICROWAVE TRANSMISSION LINES: Introduction, transmission lines equations and solutions, reflection and transmission coefficients, standing waves and SWR, line impedance and line admittance. Smith chart, impedance matching using single stubs, Microwave coaxial connectors.

7 Hours

UNIT - 2
MICROWAVE WAVEGUIDES AND COMPONENTS: Introduction, rectangular waveguides, circular waveguides, microwave cavities, microwave hybrid circuits, directional couplers, circulators and isolators.

6 Hours

UNIT - 3
MICROWAVE DIODES.
Transfer electron devices: Introduction, GUNN effect diodes – GaAs diode, RWH theory, Modes of operation, Avalanche transit time devices: READ diode, IMPATT diode, BARITT diode, Parametric amplifiers
Other diodes: PIN diodes, Schottky barrier diodes.

7 Hours
UNIT - 4
Microwave network theory and passive devices. Symmetrical Z and Y parameters, for reciprocal Networks, S matrix representation of multi port networks.  

6 Hours

PART – B

UNIT - 5
Microwave passive devices, Coaxial connectors and adapters, Phase shifters, Attenuators, Waveguide Tees, Magic tees.  

6 Hours

UNIT - 6
STRIP LINES: Introduction, Microstrip lines, Parallèle strip lines, Coplanar strip lines, Shielded strip Lines.  

6 Hours

UNIT - 7
AN INTRODUCTION TO RADAR: Basic Radar, The simple form of the Radar equation, Radar block diagram, Radar frequencies, application of Radar, the origins of Radar.  

7 Hours

UNIT - 8
MTI AND PULSE DOPPLER RADAR: Introduction to Doppler and MTI Radar, delay line Cancellers, digital MTI processing, Moving target detector, pulse Doppler Radar.  

7 Hours

TEXT BOOKS:
1. Microwave Devices and circuits- Liao / Pearson Education.  

REFERENCE BOOK:
PART – A

UNIT - 1
INFORMATION THEORY: Introduction, Measure of information, Average information content of symbols in long independent sequences, Average information content of symbols in long dependent sequences. Mark-off statistical model for information source, Entropy and information rate of mark-off source. 7 Hours

UNIT - 2
SOURCE CODING: Encoding of the source output, Shannon’s encoding algorithm. Communication Channels, Discrete communication channels, Continuous channels. 6 Hours

UNIT - 3
FUNDAMENTAL LIMITS ON PERFORMANCE: Source coding theorem, Huffman coding, Discrete memory less Channels, Mutual information, Channel Capacity. 7 Hours

UNIT - 4
Channel coding theorem, Differential entropy and mutual information for continuous ensembles, Channel capacity Theorem. 6 Hours

PART – B

UNIT - 5
INTRODUCTION TO ERROR CONTROL CODING: Introduction, Types of errors, examples, Types of codes Linear Block Codes: Matrix description, Error detection and correction, Standard arrays and table look up for decoding. 7 Hours

UNIT - 6
Binary Cycle Codes, Algebraic structures of cyclic codes, Encoding using an (n-k) bit shift register, Syndrome calculation. BCH codes. 6 Hours
UNIT - 7
RS codes, Golay codes, Shortened cyclic codes, Burst error correcting codes.
Burst and Random Error correcting codes.  
**7 Hours**

UNIT - 8
Convolution Codes, Time domain approach. Transform domain approach. 
**6 Hours**

TEXT BOOKS:

REFERENCE BOOKS:
2. Digital Communications - Glover and Grant; Pearson Ed. 2nd Ed 2008.

**FUNDAMENTALS OF CMOS VLSI**

<table>
<thead>
<tr>
<th>Subject Code</th>
<th>IA Marks</th>
</tr>
</thead>
<tbody>
<tr>
<td>10EC56</td>
<td>25</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>No. of Lecture Hrs/Week</th>
<th>Exam Hours</th>
</tr>
</thead>
<tbody>
<tr>
<td>04</td>
<td>03</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Total no. of Lecture Hrs.</th>
<th>Exam Marks</th>
</tr>
</thead>
<tbody>
<tr>
<td>52</td>
<td>100</td>
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</table>

**PART – A**

UNIT - 1
**BASIC MOS TECHNOLOGY:** Integrated circuit’s era. Enhancement and depletion mode MOS transistors. nMOS fabrication. CMOS fabrication. Thermal aspects of processing. BiCMOS technology. Production of E-beam masks. 
**3 Hours**

**4 Hours**
UNIT - 2

Basic Physical Design of Simple logic gates.  **3 Hours**

UNIT - 3
CMOS LOGIC STRUCTURES: CMOS Complementary Logic, Bi CMOS Logic, Pseudo-nMOS Logic, Dynamic CMOS Logic, Clocked CMOS Logic, Pass Transistor Logic, CMOS Domino Logic Cascaded Voltage Switch Logic (CVSL).  **6 Hours**

UNIT - 4

SCALING OF MOS CIRCUITS: Scaling models and factors. Limits on scaling. Limits due to current density and noise.  **3 Hours**

PART – B

UNIT - 5
CMOS SUBSYSTEM DESIGN: Architectural issues. Switch logic. Gate logic. Design examples – combinational logic. Clocked circuits. Other system considerations.  **5 Hours**

Clocking Strategies  **2 Hours**

UNIT - 6

UNIT - 7
MEMORY, REGISTERS AND CLOCK: Timing considerations. Memory elements. Memory cell arrays.  **6 Hours**
UNIT - 8

7 Hours

TEXT BOOKS:

REFERENCE BOOKS:

DIGITAL SIGNAL PROCESSING LABORATORY

<table>
<thead>
<tr>
<th>Subject Code</th>
<th>IA Marks</th>
<th>No. of Practical Hrs/Week</th>
<th>Exam Hours</th>
<th>Total no. of Practical Hrs.</th>
</tr>
</thead>
<tbody>
<tr>
<td>10ECL57</td>
<td>25</td>
<td>03</td>
<td>03</td>
<td>42</td>
</tr>
</tbody>
</table>

A LIST OF EXPERIMENTS USING MATLAB / SCILAB / OCTAVE / WAB

3. Verification of Sampling theorem.
4. Impulse response of a given system
5. Linear convolution of two given sequences.
6. Circular convolution of two given sequences
7. Autocorrelation of a given sequence and verification of its properties.
8. Cross correlation of given sequences and verification of its properties.
9. Solving a given difference equation.
10. Computation of N point DFT of a given sequence and to plot magnitude and phase spectrum.
11. Linear convolution of two sequences using DFT and IDFT.
12. Circular convolution of two given sequences using DFT and IDFT.
13. Design and implementation of FIR filter to meet given specifications.
14. Design and implementation of IIR filter to meet given specifications.

B. LIST OF EXPERIMENTS USING DSP PROCESSOR
1. Linear convolution of two given sequences.
2. Circular convolution of two given sequences.
3. Computation of N-Point DFT of a given sequence.
4. Realization of an FIR filter (any type) to meet given specifications. The input can be a signal from function generator / speech signal.
5. Audio applications such as to plot time and frequency (Spectrum) display of Microphone output plus a cosine using DSP. Read a wav file and match with their respective spectrograms.
6. Noise: Add noise above 3kHz and then remove; Interference suppression using 400 Hz tone.
7. Impulse response of first order and second order system.

REFERENCE BOOKS:
1. Digital signal processing using MATLAB - Sanjeet Mitra, TMH, 2001
2. Digital signal processing using MATLAB - J. G. Proakis & Ingale, MGH, 2000
3. Digital Signal Processors, B. Venkataramani and Bhaskar, TMH, 2002

ANALOG COMMUNICATION LAB + LIC LAB
Subject Code : 10ECL58
IA Marks : 25
No. of Practical Hrs/Week : 03
Exam Marks : 50
Total no. of Practical Hrs. : 42
Exam Hours : 03

EXPERIMENTS USING DESCERTE COMPONENTS and LABVIEW - 2009 CAN BE USED FOR VERIFICATION AND TESTING.
1. Second order active LPF and HPF
2. Second order active BPF and BE
3. Schmitt Trigger Design and test a Schmitt trigger circuit for the given values of UTP and LTP

45
4. Frequency synthesis using PLL.
5. Design and test R-2R DAC using op-amp
6. Design and test the following circuits using IC 555
   a. Astable multivibrator for given frequency and duty cycle
   b. Monostable multivibrator for given pulse width W
7. IF amplifier design
8. Amplitude modulation using transistor/FET (Generation and detection)
9. Pulse amplitude modulation and detection
10. PWM and PPM
11. Frequency modulation using 8038/2206
12. Precision rectifiers – both Full Wave and Half Wave.
PART – A

UNIT - 1
Basic signal processing operations in digital communication. Sampling
Principles: Sampling Theorem, Quadrature sampling of Band pass signal,
Practical aspects of sampling and signal recovery. 7 Hours

UNIT - 2
PAM, TDM. Waveform Coding Techniques, PCM, Quantization noise and
SNR, robust quantization. 6 Hours

UNIT - 3
DPCM, DM, applications. Base-Band Shaping for Data Transmission,
Discrete PAM signals, power spectra of discrete PAM signals. 7 Hours

UNIT - 4
ISI, Nyquist’s criterion for distortion less base-band binary transmission,
correlative coding, eye pattern, base-band M-ary PAM systems, adaptive
equalization for data transmission. 6 Hours

PART – B

UNIT - 5
DIGITAL MODULATION TECHNIQUES: Digital Modulation formats,
Coherent binary modulation techniques, Coherent quadrature modulation
techniques. Non-coherent binary modulation techniques. 6 Hours

UNIT - 6
Detection and estimation, Model of DCS, Gram-Schmidt Orthogonalization
procedure, geometric interpretation of signals, response of bank of correlators
to noisy input. 6 Hours

UNIT - 7
Detection of known signals in noise, correlation receiver, matched filter
receiver, detection of signals with unknown phase in noise. 7 Hours
UNIT - 8
Spread Spectrum Modulation: Pseudo noise sequences, notion of spread spectrum, direct sequence spread spectrum, coherent binary PSK, frequency hop spread spectrum, applications.  

TEXT BOOK:

REFERENCE BOOKS:
1. Digital and Analog communication systems, Simon Haykin, John Wildy India Lts, 2008

MICROPROCESSOR

<table>
<thead>
<tr>
<th>Subject Code</th>
<th>IA Marks</th>
</tr>
</thead>
<tbody>
<tr>
<td>10EC62</td>
<td>25</td>
</tr>
<tr>
<td>No. of Lecture Hrs/Week</td>
<td>Exam Hours</td>
</tr>
<tr>
<td>04</td>
<td>03</td>
</tr>
<tr>
<td>Total no. of Lecture Hrs.</td>
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</tr>
<tr>
<td>52</td>
<td>100</td>
</tr>
</tbody>
</table>

PART – A

UNIT - 1
8086 PROCESSORS: Historical background, The microprocessor-based personal computer system, 8086 CPU Architecture, Machine language instructions, Instruction execution timing.

UNIT - 2
INSTRUCTION SET OF 8086: Assembler instruction format, data transfer and arithmetic, branch type, loop, NOP & HALT, flag manipulation, logical and shift and rotate instructions. Illustration of these instructions with example programs, Directives and operators.

UNIT - 3
BYTE AND STRING MANIPULATION: String instructions, REP Prefix, Table translation, Number format conversions, Procedures, Macros, Programming using keyboard and video display.

UNIT - 4
8086 INTERRUPTS: 8086 Interrupts and interrupt responses, Hardware interrupt applications, Software interrupt applications, Interrupt examples.
PART – B

UNIT - 5
8086 INTERFACING: Interfacing microprocessor to keyboard (keyboard types, keyboard circuit connections and interfacing, software keyboard interfacing, keyboard interfacing with hardware), Interfacing to alphanumeric displays (interfacing LED displays to microcomputer), Interfacing a microcomputer to a stepper motor.  
7 Hours

UNIT - 6
8086 BASED MULTIPROCESSING SYSTEMS: Coprocessor configurations, The 8087 numeric data processor: data types, processor architecture, instruction set and examples.  
6 Hours

UNIT - 7
SYSTEM BUS STRUCTURE: Basic 8086 configurations: minimum mode, maximum mode, Bus Interface: peripheral component interconnect (PCI) bus, the parallel printer interface (LPT), the universal serial bus (USB)  
6 Hours

UNIT - 8
80386, 80486 AND PENTIUM PROCESSORS: Introduction to the 80386 microprocessor, Special 80386 registers, Introduction to the 80486 microprocessor, Introduction to the Pentium microprocessor.  
7 Hours

TEXT BOOKS:
2. The Intel Microprocessor, Architecture, Programming and Interfacing-Barry B. Brey, 6e, Pearson Education / PHI, 2003

REFERENCE BOOKS:
PART – A

UNIT – 1
MOSFETS: Device Structure and Physical Operation, V-I Characteristics, MOSFET Circuits at DC, Biasing in MOS amplifier Circuits, Small Signal Operation and Models, MOSFET as an amplifier and as a switch, biasing in MOS amplifier circuits, small signal operation modes, single stage MOS amplifiers. MOSFET internal capacitances and high frequency modes, Frequency response of CS amplifiers, CMOS digital logic inverter, detection type MOSFET.

7 Hours

UNIT -2
Single Stage IC Amplifier: IC Design philosophy, Comparison of MOSFET and BJT, Current sources, Current mirrors and Current steering circuits, high frequency response.

6 Hours

UNIT – 3
Single Stage IC amplifiers (continued): CS and CF amplifiers with loads, high frequency response of CS and CF amplifiers, CG and CB amplifiers with active loads, high frequency response of CG and CB amplifiers, Cascade amplifiers. CS and CE amplifiers with source (emitter) degeneration source and emitter followers, some useful transfer parings, current mirrors with improved performance. SPICE examples.

6 Hours

UNIT – 4
Differences and Multistage Amplifiers: The MOS differential pair, small signal operation of MOS differential pair, the BJT differences pair, other non-ideal characteristics and differential pair, Differential amplifier with active loads, frequency response and differential amplifiers. Multistage amplifier. SPICE examples.

7 Hours

PART – B

UNIT – 5
Stability problem. Effect of feedback on amplifier poles. Stability study using Bode plots. Frequency compensation. SPICE examples. 7 Hours

UNIT - 6
Operational Amplifiers: The two-stage CMOS Op-amp, folded cascade CMOS op-amp, 741 op-amp circuit, DC analysis of the 741, small signal analysis of 741, gain, frequency response and slew rate of 741. Data Converters. A-D and D-A converters. 6 Hours

UNIT – 7 & 8

TEXT BOOK:

REFERENCE BOOK:
2. “Microelectronics – Analysis and Design”, Sundaram Natarajan,

ANTENNAS AND PROPAGATION

<table>
<thead>
<tr>
<th>Subject Code</th>
<th>IA Marks</th>
<th>No. of Lecture Hrs/Week</th>
<th>Exam Hours</th>
<th>Total no. of Lecture Hrs.</th>
<th>Exam Marks</th>
</tr>
</thead>
<tbody>
<tr>
<td>10EC64</td>
<td>25</td>
<td>04</td>
<td>03</td>
<td>52</td>
<td>100</td>
</tr>
</tbody>
</table>

PART – A

UNIT - 1
ANTENNA BASICS: Introduction, basic Antenna parameters, patterns, beam area, radiation intensity, beam efficiency, diversity and gain, antenna apertures, effective height, bandwidth, radiation, efficiency, antenna temperature and antenna filed zones. 7 Hours
UNIT - 2
POINT SOURCES AND ARRAYS: Introduction, point sources, power patterns, power theorem, radiation intensity, filed patterns, phase patterns. Array of two isotropic point sources. Endfire array and Broadside array.

6 Hours

UNIT - 3
ELECTRIC DIPOLES AND THIN LINEAR ANTENNAS: Introduction, short electric dipole, fields of a short dipole(no derivation of field components), radiation resistance of short dipole, radiation resistances of lambda/2 Antenna, thin linear antenna, micro strip arrays, low side lobe arrays, long wire antenna, folded dipole antennas.

7 Hours

UNIT - 4
LOOP, SLOT, PATCH AND HORN ANTENNA: Introduction, small loop, comparison of far fields of small loop and short dipole, loop antenna general case, far field patterns of circular loop, radiation resistance, directivity, slot antenna, Babinet’s principle and complementary antennas, impedance of complementary and slot antennas, patch antennas.

8 Hours

PART – B

UNIT – 5 & 6
ANTENNA TYPES: Horn antennas, rectangular horn antennas, Helical Antenna, Yagi-Uda array, corner reflectors, parabolic reflectors, log periodic antenna, lens antenna, antenna for special applications – sleeve antenna, turnstile antenna, omni directional antennas, antennas for satellite antennas for ground penetrating radars, embedded antennas, ultra wide band antennas, plasma antenna, high-resolution data, intelligent antennas, antenna for remote sensing.

12 Hours

UNIT - 7 & 8
RADIO WAVE PROPAGATION: Introduction, Ground wave propagation, free space propagation, ground reflection, surface wave, diffraction.
TROPOSPHERE WAVE PROPAGATION: Troposcopic scatter, Ionosphere propagation, electrical properties of the ionosphere, effects of earth’s magnetic field.

10 Hours
TEXT BOOKS:

REFERENCE BOOKS:

OPERATING SYSTEMS

Subject Code : 10EC65 IA Marks : 25
No. of Lecture Hrs/Week : 04 Exam Hours : 03
Total no. of Lecture Hrs. : 52 Exam Marks : 100

PART – A

UNIT - 1
INTRODUCTION AND OVERVIEW OF OPERATING SYSTEMS:
Operating system, Goals of an O.S, Operation of an O.S, Resource allocation and related functions, User interface related functions, Classes of operating systems, O.S and the computer system, Batch processing system, Multi programming systems, Time sharing systems, Real time operating systems, distributed operating systems. 6 Hours

UNIT - 2
STRUCTURE OF THE OPERATING SYSTEMS: Operation of an O.S, Structure of the supervisor, Configuring and installing of the supervisor, Operating system with monolithic structure, layered design, Virtual machine operating systems, Kernel based operating systems, and Microkernel based operating systems. 7 Hours
UNIT - 3
PROCESS MANAGEMENT: Process concept, Programmer view of processes, OS view of processes, Interacting processes, Threads, Processes in UNIX, Threads in Solaris. 6 Hours

UNIT - 4
MEMORY MANAGEMENT: Memory allocation to programs, Memory allocation preliminaries, Contiguous and noncontiguous allocation to programs, Memory allocation for program controlled data, kernel memory allocation. 7 Hours

PART – B

UNIT - 5
VIRTUAL MEMORY: Virtual memory basics, Virtual memory using paging, Demand paging, Page replacement, Page replacement policies, Memory allocation to programs, Page sharing, UNIX virtual memory. 6 Hours

UNIT - 6
FILE SYSTEMS: File system and IOCS, Files and directories, Overview of I/O organization, Fundamental file organizations, Interface between file system and IOCS, Allocation of disk space, Implementing file access, UNIX file system. 7 Hours

UNIT - 7
SCHEDULING: Fundamentals of scheduling, Long-term scheduling, Medium and short term scheduling, Real time scheduling, Process scheduling in UNIX. 6 Hours

UNIT - 8
MESSAGE PASSING: Implementing message passing, Mailboxes, Inter process communication in UNIX. 7 Hours

TEXT BOOK:

REFERENCE BOOK:
**ADVANCED COMMUNICATION LAB**

<table>
<thead>
<tr>
<th>Subject Code</th>
<th>IA Marks</th>
</tr>
</thead>
<tbody>
<tr>
<td>10ECL67</td>
<td>25</td>
</tr>
<tr>
<td>No. of Practical Hrs/Week</td>
<td>Exam Hours</td>
</tr>
<tr>
<td>03</td>
<td>03</td>
</tr>
<tr>
<td>Total no. of Practical Hrs.: 42</td>
<td>Exam Marks</td>
</tr>
<tr>
<td>50</td>
<td>50</td>
</tr>
</tbody>
</table>

**LIST OF EXPERIMENTS USING DESCERTE COMPONENTS and LABVIEW – 2009 can be used for verification and testing.**

1. TDM of two band limited signals.
2. ASK and FSK generation and detection
3. PSK generation and detection
4. DPSK generation and detection
5. QPSK generation and detection
6. PCM generation and detection using a CODEC Chip
7. Measurement of losses in a given optical fiber (propagation loss, bending loss) and numerical aperture
8. Analog and Digital (with TDM) communication link using optical fiber.
9. Measurement of frequency, guide wavelength, power, VSWR and attenuation in a microwave test bench
10. Measurement of directivity and gain of antennas: Standard dipole (or printed dipole), microstrip patch antenna and Yagi antenna (printed).
11. Determination of coupling and isolation characteristics of a stripline (or microstrip) directional coupler
12. (a) Measurement of resonance characteristics of a microstrip ring resonator and determination of dielectric constant of the substrate.
    (b) Measurement of power division and isolation characteristics of a microstrip 3 dB power divider.

**MICROPROCESSOR LAB**

<table>
<thead>
<tr>
<th>Subject Code</th>
<th>IA Marks</th>
</tr>
</thead>
<tbody>
<tr>
<td>10ECL68</td>
<td>25</td>
</tr>
<tr>
<td>No. of Practical Hrs/Week</td>
<td>Exam Hours</td>
</tr>
<tr>
<td>03</td>
<td>03</td>
</tr>
<tr>
<td>Total no. of Practical Hrs.: 42</td>
<td>Exam Marks</td>
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<td>50</td>
<td>50</td>
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</table>

1) **Programs involving**

   1) Data transfer instructions like:
      i) Byte and word data transfer in different addressing modes.
ii] Block move (with and without overlap)
iii] Block interchange

2) Arithmetic & logical operations like:
   i] Addition and Subtraction of multi precision nos.
   ii] Multiplication and Division of signed and unsigned
       Hexa decimal nos.
   iii] ASCII adjustment instructions
   iv] Code conversions
   v] Arithmetic programs to find square cube, LCM, GCD,
       factorial

3) Bit manipulation instructions like checking:
   i] Whether given data is positive or negative
   ii] Whether given data is odd or even
   iii] Logical 1's and 0's in a given data
   iv] 2 out 5 code
   v] Bit wise and nibble wise palindrome

4) Branch/Loop instructions like:
   i] Arrays: addition/subtraction of N nos.
       Finding largest and smallest nos.
       Ascending and descending order
   ii] Near and Far Conditional and Unconditional jumps,
       Calls and Returns

5) Programs on String manipulation like string transfer, string
   reversing, searching for a string, etc.

6) Programs involving Software interrupts
   Programs to use DOS interrupt INT 21h Function calls for
   Reading a Character from keyboard, Buffered Keyboard input,
   Display of character/ String on console

II) Experiments on interfacing 8086 with the following interfacing modules
through DIO (Digital Input/Output-PCI bus compatible) card
   a] Matrix keyboard interfacing
   b] Seven segment display interface
   c] Logical controller interface
   d] Stepper motor interface

III) Other Interfacing Programs
   a] Interfacing a printer to an X86 microcomputer
   b] PC to PC Communication
ELECTIVE – I (GROUP A)
ANALOG AND MIXED MODE VLSI DESIGN

Subject Code : 10EC661 IA Marks : 25
No. of Lecture Hrs/Week : 04 Exam Hours : 03
Total no. of Lecture Hrs. : 52 Exam Marks : 100

UNIT 1

7 Hours

UNIT 2
Data Converters Architectures: DAC Architectures, Digital Input Code, Resistors String, R-2R Ladder Networks, Current Steering, Charge Scaling DACs, Cyclic DAC, Pipeline DAC, ADC Architectures, Flash, 2-Step Flash ADC, Pipeline ADC, Integrating ADC, Successive Approximation ADC.

12 Hours

UNIT 3
Non-Linear Analog Circuits: Basic CMOS Comparator Design (Excluding Characterization), Analog Multipliers, Multiplying Quad (Excluding Stimulation), Level Shifting (Excluding Input Level Shifting For Multiplier).

7 Hours

UNIT 4
Data Converter SNR: Improving SNR Using Averaging (Excluding Jitter & Averaging onwards), Decimating Filters for ADCs (Excluding Decimating without Averaging onwards), Interpolating Filters for DAC, Band pass and High pass Sync filters.

8 Hours

UNIT 5
Su-Microns CMOS circuit design: Process Flow, Capacitors and Resistors, MOSFET Switch (upto Bidirectional Switches), Delay and adder Elements, Analog Circuits MOSFET Biasing (upto MOSFET Transition Frequency).

10 Hours

UNIT 6
OPAmp Design (Excluding Circuits Noise onwards)

8 Hours

TEXT BOOK:

REFERENCE BOOKS:

SATELLITE COMMUNICATION
Subject Code : 10EC662 IA Marks : 25
No. of Lecture Hrs/Week : 04 Exam Hours : 03
Total no. of Lecture Hrs. : 52 Exam Marks : 100

PART – A

UNIT - 1
OVER VIEW OF SATELLITE SYSTEMS: Introduction, frequency allocation, INTEL Sat. 6 Hours

UNIT - 2
ORBITS: Introduction, Kepler laws, definitions, orbital element, apogee and perigee heights, orbit perturbations, inclined orbits, calendars, universal time, sidereal time, orbital plane, local mean time and sun synchronous orbits, Geostationary orbit: Introduction, antenna, look angles, polar mix antenna, limits of visibility, earth eclipse of satellite, sun transit outage, leading orbits. 7 Hours

UNIT - 3
PROPAGATION IMPAIRMENTS AND SPACE LINK: Introduction, atmospheric loss, ionospheric effects, rain attenuation, other impairments. SPACE LINK: Introduction, EIRP, transmission losses, link power budget, system noise, CNR, uplink, down link, effects of rain, combined CNR. 7 Hours

UNIT - 4
SPACE SEGMENT: Introduction, power supply units, altitude control, station keeping, thermal control, TT&C, transponders, antenna subsystem. 6 Hours

58
PART – B

UNIT - 5 & 6
EARTH SEGEMENT: Introduction, receive only home TV system, outdoor unit, indoor unit, MATV, CATV, Tx – Rx earth station. 5 Hours

INTERFERENCE AND SATELLITE ACCESS: Introduction, interference between satellite circuits, satellite access, single access, pre-assigned FDMA, SCPC (spade system), TDMA, pre-assigned TDMA, demand assigned TDMA, down link analysis, comparison of uplink power requirements for TDMA & FDMA, on board signal processing satellite switched TDMA. 9 Hours

UNIT - 7 & 8
DBS, SATELLITE MOBILE AND SPECIALIZED SERVICES: Introduction, orbital spacing, power ratio, frequency and polarization, transponder capacity, bit rates for digital TV, satellite mobile services, USAT, RadarSat, GPS, orb communication and Indian Satellite systems. 12 Hours

TEXT BOOK:

REFERENCES BOOKS:

RANDOM PROCESSES

<table>
<thead>
<tr>
<th>Subject Code</th>
<th>IA Marks</th>
</tr>
</thead>
<tbody>
<tr>
<td>10EC663</td>
<td>25</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>No. of Lecture Hrs/Week</th>
<th>Exam Hours</th>
</tr>
</thead>
<tbody>
<tr>
<td>04</td>
<td>03</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Total no. of Lecture Hrs.</th>
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</tr>
</thead>
<tbody>
<tr>
<td>52</td>
<td>100</td>
</tr>
</tbody>
</table>

PART – A

UNIT - 1
INTRODUCTION TO PROBABILITY THEORY: Experiments, sample space, Events, Axioms, Assigning probabilities, Joint and conditional
probabilities, Baye’s Theorem, Independence, Discrete Random Variables, Engg Example. 7 Hours

UNIT - 2
Random Variables, Distributions, Density Functions: CDF, PDF, Gaussian random variable, Uniform Exponential, Laplace, Gamma, Erlang, Chi-Square, Raleigh, Rician and Cauchy types of random variables. 6 Hours

UNIT - 3
OPERATIONS ON A SINGLE R V: Expected value, EV of Random variables, EV of functions of Random variables, Central Moments, Conditional expected values. 7 Hours

UNIT - 4
Characteristic functions, Probability generating functions, Moment generating functions, Engg applications, Scalar quantization, entropy and source coding. 6 Hours

PART – B

UNIT - 5
Pairs of Random variables, Joint CDF, joint PDF, Joint probability mass functions, Conditional Distribution, density and mass functions, EV involving pairs of Random variables, Independent Random variables, Complex Random variables, Engg Application. 7 Hours

UNIT - 6
MULTIPLE RANDOM VARIABLES: Joint and conditional PMF, CDF, PDF, EV involving multiple Random variables, Gaussian Random variable in multiple dimension, Engg application, linear prediction. 6 Hours

UNIT - 7
RANDOM PROCESS: Definition and characterization, Mathematical tools for studying Random Processes, Stationary and Ergodic Random processes, Properties of ACF. 6 Hours

UNIT - 8
EXAMPLE PROCESSES: Markov processes, Gaussian Processes, Poisson Processes, Engg application, Computer networks, Telephone networks. 7 Hours
TEXT BOOK:

REFERENCE BOOKS:

LOW POWER VLSI DESIGN

<table>
<thead>
<tr>
<th>Subject Code</th>
<th>: 10EC664</th>
<th>IA Marks  : 25</th>
</tr>
</thead>
<tbody>
<tr>
<td>No. of Lecture Hrs/Week</td>
<td>: 04</td>
<td>Exam Hours : 03</td>
</tr>
<tr>
<td>Total no. of Lecture Hrs.</td>
<td>: 52</td>
<td>Exam Marks : 100</td>
</tr>
</tbody>
</table>

PART – A

UNIT – 1
Introduction, Sources of power dissipation, designing for low power. Physics of power dissipation in MOSFET devices – MIS Structure, Long channel and sub-micron MOSFET, Gate induced Drain leakage. **6 Hours**

UNIT - 2
Power dissipation in CMOS – Short circuit dissipation, dynamic dissipation, Load capacitance. Low power design limits - Principles of low power design, Hierarchy of limits, fundamental limits, Material, device, circuit and system limits. **8 Hours**

UNIT – 3&4
SYNTHESIS FOR LOW POWER: Behavioral, Logic and Circuit level approaches, Algorithm level transforms, Power-constrained Least squares optimization for adaptive and non-adaptive filters, Circuit activity driven architectural transformations, voltage scaling, operation reduction and substitution, pre- computation, FSM and Combinational logic, Transistor sizing. **12 Hours**
PART – B

UNIT – 5&6
DESIGN AND TEST OF LOW-VOLTAGE CMOS CIRCUITS:
Introduction, Design style, Leakage current in Deep sub-micron transistors, device design issues, minimizing short channel effect, Low voltage design techniques using reverse $V_{gs}$, steep sub threshold swing and multiple threshold voltages, Testing with elevated intrinsic leakage, multiple supply voltages. 12 Hours

UNIT - 7
LOW ENERGY COMPUTING: Energy dissipation in transistor channel, Energy recovery circuit design, designs with reversible and partially reversible logic, energy recovery in adiabatic logic and SRAM core, Design of peripheral circuits – address decoder, level shifter and I/O Buffer, supply clock generation. 7 Hours

UNIT - 8
SOFTWARE DESIGN FOR LOW POWER: Introduction, sources of power dissipation, power estimation and optimization. 7 Hours

TEXT BOOK:

DATA STRUCTURE USING C++

<table>
<thead>
<tr>
<th>Subject Code</th>
<th>IA Marks</th>
</tr>
</thead>
<tbody>
<tr>
<td>10EC665</td>
<td>25</td>
</tr>
<tr>
<td>No. of Lecture Hrs/Week</td>
<td>Exam Hours</td>
</tr>
<tr>
<td>04</td>
<td>03</td>
</tr>
<tr>
<td>Total no. of Lecture Hrs.</td>
<td>Exam Marks</td>
</tr>
<tr>
<td>52</td>
<td>100</td>
</tr>
</tbody>
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PART – A

UNIT - 1
INTRODUCTION: Functions and parameters, Dynamic memory allocation classis, Testing and debugging. Data Representation, Introduction, Linear lists, Formula-based representation linked representation, Indirect addressing simulating pointers. 7 Hours
UNIT - 2
ARRAYS AND MATRICES: Arrays, Matrices, Special matrices spare matrices. 6 Hours

UNIT - 3
STACKS: The abstract data types, Derived classes and inheritance, Formula-based representation, Linked representation, Applications. 7 Hours

UNIT - 4
Queues: The abstract data types, Derived classes and inheritance, Formula-based representation, Linked Linked representation, Applications. 6 Hours

PART – B

UNIT - 5
SKIP LISTS AND HASHING: Dictionaries, Linear representation, Skip list presentation, Hash table representation. 6 Hours

UNIT - 6
BINARY AND OTHER TREES: Trees, Binary trees, Properties and representation of binary trees, Common binary tree operations, Binary tree traversal the ADT binary tree, ADT and class extensions. 8 Hours

UNIT - 7
PRIIRITY QUEUES: Linear lists, Heaps, Leftist trees. 6 Hours

UNIT-8
Search Trees: Binary search trees, B-trees, Applications. 6 Hours

TEXT BOOK:
2. REFERENCE BOOKS:
PART – A

UNIT 1
Introduction and Methodology:
Digital Systems and Embedded Systems, Binary representation and Circuit Elements, Real-World Circuits, Models, Design Methodology.  
7 Hours

UNIT 2
Combinational Basics:
Boolean Functions and Boolean Algebra, Binary Coding, Combinational Components and Circuits, Verification of Combinational Circuits.  
7 Hours

UNIT 3
Number Basics:
Unsigned and Signed Integers, Fixed and Floating-point Numbers.  
6 Hours

UNIT 4
Sequential Basics: Storage elements, Counters, Sequential Datapaths and Control, Clocked Synchronous Timing Methodology.  
6 Hours

PART – B

UNIT 5
Memories: Concepts, Memory Types, Error Detection and Correction. Implementation Fabrics: ICs, PLDs, Packaging and Circuit Boards, Interconnection and Signal Integrity.  
7 Hours

UNIT 6
Processor Basics: Embedded Computer Organization, Instruction and Data, Interfacing with memory.  
6 Hours

UNIT 7
I/O interfacing: I/O devices, I/O controllers, Parallel Buses, Serial Transmission, I/O software.  
6 Hours
UNIT 8
Accelerators: Concepts, case study, Verification of accelerators.

Design Methodology: Design flow, Design optimization, Design for test.

7 Hours

TEXT BOOK:

VIRTUAL INSTRUMENTATION

<table>
<thead>
<tr>
<th>Subject Code</th>
<th>IA Marks</th>
</tr>
</thead>
<tbody>
<tr>
<td>10EC667</td>
<td>25</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>No. of Lecture Hrs/Week</th>
<th>Exam Hours</th>
</tr>
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<tbody>
<tr>
<td>04</td>
<td>03</td>
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</tbody>
</table>

<table>
<thead>
<tr>
<th>Total no. of Lecture Hrs.</th>
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<tr>
<td>52</td>
<td>100</td>
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PART – A

UNIT 1
Review of Digital Instrumentation: Representation of analog signals in the digital domain – Review of quantization in amplifier and time areas, sample and hold, sampling theorem, ADC and DAC.

8 Hours

UNIT 2 & 3

12 Hours

UNIT 4

8 Hours
PART – B

UNIT 5 & 6

Graphical Programming Environment in VI:
Concepts of graphical programming – Lab-view software – Concept of VIs and sub VIs – Display types – Digital – Analog – Chart – Oscilloscope types – Loops – Case and sequence structures – Types of data – Arrays – Formulate nodes – Local and Global variables – String and file I/O.

12 Hours

UNIT 7 & 8

Analysis Tools and Simple Application in VI:

12 Hours

TEXT BOOKS:

REFERENCE BOOKS:
PART – A

UNIT - 1
Layered tasks, OSI Model, Layers in OSI model, TCP/IP Suite, Addressing, Telephone and cable networks for data transmission, Telephone networks, Dial up modem, DSL, Cable TV for data transmission. 7 Hours

UNIT - 2
DATA LINK CONTROL: Framing, Flow and error control, Protocols, Noiseless channels and noisy channels, HDLC. 6 Hours

UNIT - 3
MULTIPLE ACCESSES: Random access, Controlled access, Channelisation. 6 Hours

UNIT - 4
Wired LAN, Ethernet, IEEE standards, Standard Ethernet. Changes in the standards, Fast Ethernet, Gigabit Ethernet, Wireless LAN IEEE 802.11 7 Hours

PART – B

UNIT - 5
Connecting LANs, Backbone and Virtual LANs, Connecting devices, Backbone Networks, Virtual LANs 7 Hours

UNIT - 6
Network Layer, Logical addressing, Ipv4 addresses, Ipv6 addresses, Ipv4 and Ipv6 Transition from Ipv4 to Ipv6. 6 Hours

UNIT - 7
Delivery, Forwarding, Unicast Routing Protocols, Multicast Routing protocols. 6 Hours
UNIT - 8
Transport layer Process to process Delivery, UDP, TCP, Domain name system, Resolution.  

TEXT BOOK:

REFERENCE BOOKS:

OPTICAL FIBER COMMUNICATION

<table>
<thead>
<tr>
<th>Subject Code</th>
<th>IA Marks</th>
</tr>
</thead>
<tbody>
<tr>
<td>10EC72</td>
<td>25</td>
</tr>
<tr>
<td>No. of Lecture Hrs/Week</td>
<td>Exam Hours</td>
</tr>
<tr>
<td>04</td>
<td>03</td>
</tr>
<tr>
<td>Total no. of Lecture Hrs.</td>
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</tr>
<tr>
<td>52</td>
<td>100</td>
</tr>
</tbody>
</table>

PART – A

UNIT - 1
OVERVIEW OF OPTICAL FIBER COMMUNICATION: Introduction, Historical development, general system, advantages, disadvantages, and applications of optical fiber communication, optical fiber waveguides, Ray theory, cylindrical fiber (no derivations in article 2.4.4), single mode fiber, cutoff wave length, mode filed diameter. Optical Fibers: fiber materials, photonic crystal, fiber optic cables specialty fibers.  

UNIT - 2

UNIT - 3
OPTICAL SOURCES AND DETECTORS: Introduction, LED’s, LASER diodes, Photo detectors, Photo detector noise, Response time, double hetero junction structure, Photo diodes, comparison of photo detectors.
UNIT - 4
FIBER COUPLERS AND CONNECTORS: Introduction, fiber alignment and joint loss, single mode fiber joints, fiber splices, fiber connectors and fiber couplers. 6 Hours

UNIT - 5
OPTICAL RECEIVER: Introduction, Optical Receiver Operation, receiver sensitivity, quantum limit, eye diagrams, coherent detection, burst mode receiver, operation, Analog receivers. 6 Hours

UNIT - 6
ANALOG AND DIGITAL LINKS: Analog links – Introduction, overview of analog links, CNR, multichannel transmission techniques, RF over fiber, key link parameters, Radio over fiber links, microwave photonics. Digital links – Introduction, point-to-point links, System considerations, link power budget, resistive budget, short wave length band, transmission distance for single mode fibers, Power penalties, nodal noise and chirping. 8 Hours

UNIT - 7
WDM CONCEPTS AND COMPONENTS: WDM concepts, overview of WDM operation principles, WDM standards, Mach-Zehender interferometer, multiplexer, Isolators and circulators, direct thin film filters, active optical components, MEMS technology, variable optical attenuators, tunable optical fibers, dynamic gain equalizers, optical drop multiplexers, polarization controllers, chromatic dispersion compensators, tunable light sources. 7 Hours

UNIT - 8
Optical Amplifiers and Networks – optical amplifiers, basic applications and types, semiconductor optical amplifiers, EDFA. OPTICAL NETWORKS: Introduction, SONET / SDH, Optical Interfaces, SONET/SDH rings, High – speed light – waveguides. 6 Hours

TEXT BOOKS:

REFERENCE BOOK:
PART – A

UNIT - 1
Introduction, Applications of power electronics, Power semiconductor devices, Control characteristics, Types of power electronics circuits, Peripheral effects.  

UNIT - 2
POWER TRANSISTOR: Power BJT’s, Switching characteristics, Switching limits, Base derive control, Power MOSFET’s, Switching characteristics, Gate drive, IGBT’s, Isolation of gate and base drives.

UNIT - 3
INTRODUCTION TO THYRISTORS: Principle of operation states anode-cathode characteristics, Two transistor model. Turn-on Methods, Dynamic Turn-on and turn-off characteristics, Gate characteristics, Gate trigger circuits, di / dt and dv / dt protection, Thyristor firing circuits.

UNIT - 4
CONTROLLED RECTIFIERS: Introduction, Principles of phase controlled converter operation, 1$\phi$ fully controlled converters, Duel converters, 1 $\phi$ semi converters (all converters with R & RL load).

PART – B

UNIT - 5
Thyristor turn off methods, natural and forced commutation, self commutation, class A and class B types, Complementary commutation, auxiliary commutation, external pulse commutation, AC line commutation, numerical problems.

UNIT - 6
AC VOLTAGE CONTROLLERS: Introduction, Principles of on and off control, Principles of phase control, Single phase controllers with resistive loads and Inductive loads, numerical problems.
UNIT - 7
DC CHOPPERS: Introduction, Principles of step down and step up choppers, Step down chopper with RL loads, Chopper classification, Switch mode regulators – buck, boost and buck – boost regulators. 6 Hours

UNIT - 8
INVERTORS: Introduction, Principles of operation, Performance parameters, 1φ bridge inverter, voltage control of 1φ invertors, current source invertors, Variable DC link inverter. 7 Hours

TEXT BOOKS:

REFERENCE BOOKS:

EMBEDED SYSTEM DESIGN

Subject Code : 10EC74 IA Marks : 25
No. of Lecture Hrs/Week : 04 Exam Hours : 03
Total no. of Lecture Hrs. : 52 Exam Marks : 100

PART – A

UNIT 1:
Introduction to Embedded System: Introducing Embedded Systems, Philosophy, Embedded Systems, Embedded Design and Development Process. 5 Hours

UNIT 2:
The Hardware Side: An Introduction, The Core Level, Representing Information, Understanding Numbers, Addresses, Instructions, Registers-A
First Look, Embedded Systems-An Instruction Set View, Embedded Systems-A Register View, Register View of a Microprocessor
The Hardware Side: Storage Elements and Finite-State Machines (2 hour)
The concepts of State and Time, The State Diagram, Finite State Machines- A Theoretical Model.

UNIT 3:

UNIT 4:

PART – B

UNIT 5 & 6:

UNIT 7 & 8:
Performance Analysis and Optimization: Performance or Efficiency Measures, Complexity Analysis, The methodology, Analyzing code, Instructions in Detail, Time, etc. – A more detailed look, Response Time, Time Loading, Memory Loading, Evaluating Performance, Thoughts on Performance Optimization, Performance Optimization, Tricks of the Trade, Hardware Accelerators, Caches and Performance.
TEXT BOOK:

REFERENCE BOOKS:

VLSI LAB

<table>
<thead>
<tr>
<th>Subject Code</th>
<th>IA Marks</th>
<th>No. of Practical Hrs/Week</th>
<th>Exam Hours</th>
<th>Total no. of Practical Hrs.</th>
<th>Exam Marks</th>
</tr>
</thead>
<tbody>
<tr>
<td>10ECL77</td>
<td></td>
<td>03</td>
<td>03</td>
<td>42</td>
<td>50</td>
</tr>
</tbody>
</table>

(Wherever necessary Cadence/Synopsis/Menta Graphics tools must be used)

PART - A

DIGITAL DESIGN

ASIC-DIGITAL DESIGN FLOW
1. Write Verilog Code for the following circuits and their Test Bench for verification, observe the waveform and synthesize the code with technological library with given Constraints*. Do the initial timing verification with gate level simulation.
   1. An inverter
   2. A Buffer
   3. Transmission Gate
   4. Basic/universal gates
   5. Flip flop -RS, D, JK, MS, T
   6. Serial & Parallel adder
   7. 4-bit counter [Synchronous and Asynchronous counter]
   8. Successive approximation register [SAR]

* An appropriate constraint should be given
PART - B
ANALOG DESIGN

Analog Design Flow
1. Design an **Inverter** with given specifications*, completing the design flow mentioned below:
   a. Draw the schematic and verify the following
      i) DC Analysis
      ii) Transient Analysis
   b. Draw the Layout and verify the DRC, ERC
   c. Check for LVS
   d. Extract RC and back annotate the same and verify the Design
   e. Verify & Optimize for Time, Power and Area to the given constraint***

2. Design the following circuits with given specifications*, completing the design flow mentioned below:
   a. Draw the schematic and verify the following
      i) DC Analysis
      ii) AC Analysis
      iii) Transient Analysis
   b. Draw the Layout and verify the DRC, ERC
   c. Check for LVS
   d. Extract RC and back annotate the same and verify the Design.
      i) A Single Stage differential amplifier
      ii) Common source and Common Drain amplifier

3. Design an **op-amp** with given specification* using given differential amplifier Common source and Common Drain amplifier in library** and completing the design flow mentioned below:
   a. Draw the schematic and verify the following
      i) DC Analysis
      ii). AC Analysis
      iii) Transient Analysis
   b. Draw the Layout and verify the DRC, ERC
   c. Check for LVS
   d. Extract RC and back annotate the same and verify the Design.

4. Design a **4 bit R-2R based DAC** for the given specification and completing the design flow mentioned using given op-amp in the library**.
   a. Draw the schematic and verify the following
5. For the **SAR based ADC** mentioned in the figure below draw the mixed signal schematic and verify the functionality by completing ASIC Design FLOW.

**[Specifications to GDS-II]**

![SAR based ADC schematic](image)

* Appropriate specification should be given.
** Applicable Library should be added & information should be given to the Designer.
*** An appropriate constraint should be given

**POWER ELECTRONICS LAB**

<table>
<thead>
<tr>
<th>Subject Code</th>
<th>:10ECL.78</th>
<th>IA Marks</th>
<th>: 25</th>
</tr>
</thead>
<tbody>
<tr>
<td>No. of Practical Hrs/Week:</td>
<td>03</td>
<td>Exam Hours</td>
<td>: 03</td>
</tr>
<tr>
<td>Total no. of Practical Hrs.:</td>
<td>42</td>
<td>Exam Marks</td>
<td>: 50</td>
</tr>
</tbody>
</table>

Any five converter circuits experiment from the below list must be simulated using the **spice-simulator**.

- Static characteristics of SCR and DIAC.
- Static characteristics of MOSFET and IGBT.
• Controlled HWR and FWR using RC triggering circuit
• SCR turn off using i) LC circuit ii) Auxiliary Commutation
• UJT firing circuit for HWR and FWR circuits.
• Generation of firing signals for thyristors/ trials using digital circuits / microprocessor.
• AC voltage controller using triac – diac combination.
• Single phase Fully Controlled Bridge Converter with R and R-L loads.
• Voltage (Impulse) commutated chopper both constant frequency and variable frequency operations.
• Speed control of a separately exited DC motor.
• Speed control of universal motor.
• Speed control of stepper motor.
• Parallel/ series inverter.
Note: Experiments to be conducted with isolation transformer and low voltage.

DSP ALGORITHMS AND ARCHITECTURE

<table>
<thead>
<tr>
<th>Subject Code</th>
<th>IA Marks</th>
</tr>
</thead>
<tbody>
<tr>
<td>10EC751</td>
<td>25</td>
</tr>
</tbody>
</table>

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<thead>
<tr>
<th>No. of Lecture Hrs/Week</th>
<th>Exam Hours</th>
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<tbody>
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<td>04</td>
<td>03</td>
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<thead>
<tr>
<th>Total no. of Lecture Hrs.</th>
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<td>52</td>
<td>100</td>
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PART – A

UNIT - 1

6 Hours

UNIT - 2
ARCHITECTURES FOR PROGRAMMABLE DIGITAL SIGNAL-PROCESSORS: Introduction, Basic Architectural Features, DSP Computational Building Blocks, Bus Architecture and Memory, Data Addressing Capabilities, Address Generation Unit, Programmability and Program Execution, Features for External Interfacing.  

7 Hours

UNIT - 3
PROGRAMMABLE DIGITAL SIGNAL PROCESSORS: Introduction, Commercial Digital Signal-processing Devices, Data Addressing Modes of
UNIT - 4
Detail Study of TMS320C54X & 54xx Instructions and Programming, On-Chip peripherals, Interrupts of TMS320C54XX Processors, Pipeline Operation of TMS320C54xx Processor. 7 Hours

PART – B

UNIT - 5
IMPLEMENTATION OF BASIC DSP ALGORITHMS: Introduction, The Q-notation, FIR Filters, IIR Filters, Interpolation and Decimation Filters (one example in each case). 7 Hours

UNIT - 6
IMPLEMENTATION OF FFT ALGORITHMS: Introduction, An FFT Algorithm for DFT Computation, Overflow and Scaling, Bit-Reversed Index Generation & Implementation on the TMS320C54xx. 6 Hours

UNIT - 7
INTERFACING MEMORY AND PARALLEL I/O PERIPHERALS TO DSP DEVICES: Introduction, Memory Space Organization, External Bus Interfacing Signals, Memory Interface, Parallel I/O Interface, Programmed I/O, Interrupts and I / O Direct Memory Access (DMA). 6 Hours

UNIT - 8

TEXT BOOK:

REFERENCE BOOKS:
PART – A

UNIT - 1
INTRODUCTION TO MICRO AND SMART SYSTEMS:


UNIT - 2
MICRO AND SMART DEVICES AND SYSTEMS: PRINCIPLES AND MATERIALS:

a) Definitions and salient features of sensors, actuators, and systems.

b) Sensors: silicon capacitive accelerometer, piezo-resistive pressure sensor, blood analyzer, conductometric gas sensor, fiber-optic gyroscope and surface-acoustic-wave based wireless strain sensor.

c) Actuators: silicon micro-mirror arrays, piezo-electric based inkjet print-head, electrostatic comb-drive and micromotor, magnetic micro relay, shape-memory-alloy based actuator, electro-thermal actuator.

d) Systems: micro gas turbine, portable clinical analyzer, active noise control in a helicopter cabin. 7 Hours

UNIT - 3
MICROMANUFACTURING AND MATERIAL PROCESSING:

a. Silicon wafer processing, lithography, thin-film deposition, etching (wet and dry), wafer-bonding, and metallization.

b. Silicon micromachining: surface, bulk, moulding, bonding based process flows.

c. Thick-film processing:

d. Smart material processing:

e. Processing of other materials: ceramics, polymers and metals

f. Emerging trends. 7 Hours
UNIT - 4
MODELING:

a. Scaling issues.

6 Hours

UNIT - 5
COMPUTER-AIDED SIMULATION AND DESIGN:

6 Hours

UNIT - 6
ELECTRONICS, CIRCUITS AND CONTROL:

7 Hours

UNIT - 7
INTEGRATION AND PACKAGING OF MICROELECTRO MECHANICAL SYSTEMS:

7 Hours

UNIT - 8
CASE STUDIES:
BEL pressure sensor, thermal cycler for DNA amplification, and active vibration control of a beam.

6 Hours

UNIT - 9
Mini-projects and class-demonstrations (not for Examination)
a) CAD lab (coupled field simulation of electrostatic-elastic actuation with fluid effect)
b) BEL pressure sensor
c) Thermal-cycler for PCR
d) Active control of a cantilever beam

**TEXT BOOKS AND A CD-SUPPLEMENT:**
2. “Micro and Smart Systems” by Dr. A.K.Aatre, Prof. Ananth Suresh, Prof.K.J.Vinoy, Prof. S. Gopalakrishna,, Prof. K.N.Bhat., John Wiley Publications.

**REFERENCE BOOKS:**
1. Animations of working principles, process flows and processing techniques, A CD-supplement with Matlab codes, photographs and movie clips of processing machinery and working devices.
2. **Laboratory hardware kits for** (i) BEL pressure sensor, (ii) thermal-cycler and (iii) active control of a cantilever beam.
6. **MEMS- Nitaigour Premchand Mahalik, TMH 2007**

**ARTIFICIAL NEURAL NETWORKS**

<table>
<thead>
<tr>
<th>Subject Code</th>
<th>IA Marks</th>
</tr>
</thead>
<tbody>
<tr>
<td>10EC753</td>
<td>25</td>
</tr>
<tr>
<td>No. of Lecture Hrs/Week</td>
<td>Exam Hours</td>
</tr>
<tr>
<td>04</td>
<td>03</td>
</tr>
<tr>
<td>Total no. of Lecture Hrs.</td>
<td>Exam Marks</td>
</tr>
<tr>
<td>52</td>
<td>100</td>
</tr>
</tbody>
</table>

**PART – A**

**UNIT - 1**
Introduction, history, structure and function of single neuron, neural network architectures, neural learning, use of neural networks. **6 Hours**
UNIT - 2
Supervised learning, single layer networks, perceptions, linear separability, perceptions training algorithm, guarantees of success, modifications. 

UNIT - 3
Multiclass networks-I, multilevel discrimination, preliminaries, back propagation, setting parameter values, theoretical results. 

UNIT - 4
Accelerating learning process, application, mandaline, adaptive multilayer networks. 

PART – B

UNIT - 5
Prediction networks, radial basis functions, polynomial networks, regularization, unsupervised learning, winner take all networks. 

UNIT - 6
Learning vector quantizing, counter propagation networks, adaptive resonance theorem, topologically organized networks, distance based learning, neo-cognition. 

UNIT - 7
Associative models, hop field networks, brain state networks, Boltzmann machines, hetero associations. 

UNIT - 8
Optimization using hop filed networks, simulated annealing, random search, evolutionary computation. 

TEXT BOOK:

REFERENCE BOOKS:
UNIT – 1&2
INTRODUCTION TO VLSI METHODOLOGIES: VLSI Physical Design Automation - Design and Fabrication of VLSI Devices - Fabrication process and its impact on Physical Design. 12 Hours

UNIT – 3&4
A QUICK TOUR OF VLSI DESIGN AUTOMATION TOOLS: Data structures and Basic Algorithms, Algorithmic Graph theory and computational complexity, Tractable and Intractable problems. 14 Hours

PART – B

UNIT – 5&6
GENERAL PURPOSE METHODS FOR COMBINATIONAL OPTIMIZATION: partitioning, floor planning and pin assignment, placement, routing. 14 Hours

UNIT – 7&8
SIMULATION-LOGIC SYNTHESIS: Verification-High level synthesis - Compaction. Physical Design Automation of FPGAs, MCMS-VHDL-Verilog-Implementation of Simple circuits using VHDL and Verilog. 12 Hours

REFERENCE BOOKS:

REFERENCE BOOKS:
APPLIED EMBEDDED SYSTEM DESIGN

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<thead>
<tr>
<th>Subject Code</th>
<th>IA Marks</th>
<th>No. of Lecture Hrs/Week</th>
<th>Exam Hours</th>
<th>Total no. of Lecture Hrs.</th>
<th>Exam Marks</th>
</tr>
</thead>
<tbody>
<tr>
<td>10EC755</td>
<td>25</td>
<td>04</td>
<td>03</td>
<td>52</td>
<td>100</td>
</tr>
</tbody>
</table>

PART – A

UNIT - 1
INTRODUCTION TO THE EMBEDDED SYSTEMS: An embedded System, Processor embedded into a system (A). Embedded Hardware Units and devices in a system, Embedded software in a system, Examples of embedded systems, Embedded system-on-chip (SoC) and use of VLSI circuits design technology (A), Complex systems design and processors, Design process in embedded system, Formalism of system design, Design process and design examples, Classification of embedded systems, Skills required for an embedded system designer.

5 Hours

UNIT - 2
8051 AND ADVANCED PROCESSOR ARCHITECTURE: 8051 Architecture, Real world interfacing, Introduction to advanced architecture Processor and memory architecture, Instruction level parallelism, Performance metrics Memory types and addresses, Processor selection, Memory selection.

5 Hours

UNIT - 3
DEVICES AND COMMUNICATION BUSES FOR DEVICES NETWORK: Devices and Communication buses for Networks, Serial communication devices Parallel port devices, Sophisticated interfacing features in device ports, Wireless communication devices, Timer and counting devices, Watchdog timers, Real time clocks Parallel bus device protocols – parallel communication network using the ISA, PCI, PCI-X and advanced buses, Wireless and mobile system protocols..

6 Hours

UNIT - 4
DEVICE DRIVERS AND INTERRUPTS SERVICING MECHANISM: Port or device access without interrupt servicing mechanism, Interrupt service routine, thread and device driver concept, Interrupt sources, Interrupt servicing (handling) mechanism Multiple interrupts, Context and the periods
for context-switching, interrupt latency and Deadline Classification of processors interrupt service mechanism from context saving angle Direct memory access, Device driver programming, Parallel port device drivers in a system Serial port device drivers in a system, Timer devices and devices interrupts.

**PART – B**

**UNIT - 5**

**PROGRAMMING CONCEPTS AND EMBEDDED PROGRAMMING IN C, C++ AND JAVA:** Software programming in assembly language (ALP) and in high level language ‘C’, ‘C’ programming elements: header and source files and preprocessor directives, program elements : macros and functions, Program elements : data types, data structures, modifiers, statements, loops and pointers, Objected oriented programming, Embedded programming in Java, Optimisation of Memory needs.

5 Hours

**UNIT - 6**

**PROGRAM MODELING CONCEPTS IN SINGLE AND MULTIPROCESSOR SYSTEMS SOFTWARE – DEVELOPMENT PROCESS:** Program models, Data flow graph models, State machine programming models for event controlled programs, Modeling of multiprocessor systems, UML modeling.

5 Hours

**UNIT - 7**

**REAL TIME OPERATING SYSTEMS – 1: INTER PROCESS COMMUNICATION AND SYNCHRONISATION OF PROCESSES, TASK AND THREADS:** Multiple processes in an application, Multiple threads in an applications, Task Tasks and states, Tasks and data, Clear cut distinction between Functions, ISRs and Tasks by their Characteristics, Concept of semaphores, Shared data, Inter process communications Signals, Semaphores, Message queues, Mailboxes, Pipes, Sockets, Remote procedure calls (RPCs).

8 Hours

**UNIT - 8**

**REAL TIME OPERATING SYSTEMS:** Operating system service, Process management, Timer functions, Event functions, Memory management, Device, file and IO subsystems management Interrupt routines in RTOS environment and handling of interrupt source calls by RTOS Introduction to Real time Operating System, Basic design using a Real Time Operating System, RTOS Task Scheduling Models, Latency, Response Times, Deadline
as Performance Metric, OS security issues, IEEE Standard POSIX 1003.1 b Functions for Standardisation of RTOS an Inter Process Communication Functions, Types of Real Time Operating Systems RTOS\textsuperscript{\textmu}C/OS-II, RTOS Vx Works.

10 Hours

TEXT BOOK:

REFERENCE BOOKS:
1. Introduction to Embedded System Design – A certified Hardware / Software by Bank Vahid, John Wikey & Sons, 2002.

Lab Work: (Part of the theory class)
1. Write C prog to initialize the I/O ports and interface the following:
   a. LED / LCD Display
   b. Stepper Motor
   c. Elevator

DIGITAL CMOS CIRCUITS: Overview, Design and performance analysis of CMSO inverter, Logic Gate Circuits, Pass-transistor logic, Dynamic Logic Circuits, SPICE examples.

TEXT BOOK:

REFERENCE BOOKS:
PART – A

UNIT - 1
PRODUCTION AND CLASSIFICATION OF SPEECH SOUNDS:
Introduction, mechanism of speech production. Acoustic phonetics: vowels, diphthongs, semivowels, nasals, fricatives, stops and affricates. 6 Hours

UNIT - 2
TIME-DOMAIN METHODS FOR SPEECH PROCESSING: time dependent processing of speech, short-time energy and average magnitude, short-time average zero crossing rate. 6 Hours

UNIT - 3
Speech vs. silence detection, pitch period estimation using parallel processing approach, short-time autocorrelation function. 7 Hours

UNIT - 4
Brief Applications of temporal processing of speech signals in synthesis, enhancement, hearing applications and clear speech. 7 Hours

PART – B

UNIT - 5
FREQUENCY DOMAIN METHODS FOR SPEECH PROCESSING:
Introduction, definitions and properties: Fourier transforms interpretation and linear filter interpretation, sampling rates in time and frequency. 7 Hours

UNIT - 6
Filter bank summation and overlap add methods for short-time synthesis of speech, sinusoidal and harmonic plus noise method of analysis/synthesis. 6 Hours
UNIT - 7
HOMOMORPHIC SPEECH PROCESSING: Introduction, homomorphic system for convolution, the complex cepstrum of speech, homomorphic vocoder.  
6 Hours

UNIT - 8
APPLICATIONS OF SPEECH PROCESSING: Brief applications of speech processing in voice response systems hearing aid design and recognition systems.  
7 Hours

TEXT BOOK:

REFERENCE BOOKS:

ELECTIVE-III (GROUP-C)
PROGRAMMING IN C++

<table>
<thead>
<tr>
<th>Subject Code</th>
<th>IA Marks</th>
</tr>
</thead>
<tbody>
<tr>
<td>10EC761</td>
<td>25</td>
</tr>
<tr>
<td>No. of Lecture Hrs/Week</td>
<td>Exam Hours</td>
</tr>
<tr>
<td>04</td>
<td>03</td>
</tr>
<tr>
<td>Total no. of Lecture Hrs.</td>
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<td>52</td>
<td></td>
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</tbody>
</table>

PART – A

UNIT - 1
7 Hours

UNIT - 2
THE BASIC LANGUAGE: Literal Constant, Variables, Pointer Type, String Types, const Qualifier, Reference Types, the bool type, Enumeration types, Array types. The vector container type.  
6 Hours
UNIT - 3
OPERATORS: Arithmetic Operators, Equality, Relational and Logical operators, Assignment operators, Increment and Decrement operator, The conditional Operator, Bitwise operator, bitset operations. Statements: if, switch, for Loop, while, break, goto, continue statements.

7 Hours

UNIT - 4
FUNCTIONS: Prototype, Argument passing, Recursion and linear function.

6 Hours

PART – B

UNIT - 5
EXCEPTION HANDLING: Throwing an Exception, Catching an exception, Exception Specification and Exceptions and Design Issues.

7 Hours

UNIT - 6
CLASSES: Definition, Class Objects, Class Initailization, Class constructor, The class destructor, Class Object Arrays and Vectors.

7 Hours

UNIT - 7
Overload Operators, Operators ++ and --, Operators new and delete.

6 Hours

UNIT - 8
Multiple Inheritances, public, private & protected inheritance, Class scope under Inheritance.

6 Hours

TEXT BOOK:

REFERENCE BOOKS:
REAL-TIME SYSTEMS

Subject Code : 10EC762 IA Marks : 25
No. of Lecture Hrs/Week : 04 Exam Hours : 03
Total no. of Lecture Hrs. : 52 Exam Marks : 100

PART – A

UNIT - 1
INTRODUCTION TO REAL-TIME SYSTEMS: Historical background, RTS Definition, Classification of Real-time Systems, Time constraints, Classification of Programs. 6 Hours

UNIT - 2
CONCEPTS OF COMPUTER CONTROL: Introduction, Sequence Control, Loop control, Supervisory control, Centralised computer control, Distributed system, Human-computer interface, Benefits of computer control systems. 6 Hours

UNIT - 3
COMPUTER HARDWARE REQUIREMENTS FOR RTS: Introduction, General purpose computer, Single chip microcontroller, Specialized processors, Process-related Interfaces, Data transfer techniques, Communications, Standard Interface. 7 Hours

UNIT - 4
LANGUAGES FOR REAL-TIME APPLICATIONS: Introduction, Syntax layout and readability, Declaration and Initialization of Variables and Constants, Modularity and Variables, Compilation, Data types, Control Structure, Exception Handling, Low-level facilities, Co-routines, Interrupts and Device handling, Concurrency, Real-time support, Overview of real-time languages. 7 Hours

PART – B

UNIT - 5 & 6
OPERATING SYSTEMS: Introduction, Real-time multi-tasking OS, Scheduling strategies, Priority Structures, Task management, Scheduler and real-time clock interrupt handles, Memory Management, Code sharing, Resource control, Task co-operation and communication, Mutual exclusion, Data transfer, Liveness, Minimum OS kernel, Examples. 14 Hours
UNIT - 7
**DESIGN OF RTSS – GENERAL INTRODUCTION:** Introduction, Specification documentation, Preliminary design, Single-program approach, Foreground/background, Multi-tasking approach, Mutual exclusion, Monitors.  
*6 Hours*

UNIT - 8
**RTS DEVELOPMENT METHODOLOGIES:** Introduction, Yourdon Methodology, Requirement definition for Drying Oven, Ward and Mellor Method, Hately and Pirbhai Method.  
*6 Hours*

**TEXT BOOKS:**

**REFERENCE BOOKS:**

**IMAGE PROCESSING**

<table>
<thead>
<tr>
<th>Subject Code</th>
<th>IA Marks</th>
</tr>
</thead>
<tbody>
<tr>
<td>10EC763</td>
<td>25</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>No. of Lecture Hrs/Week</th>
<th>Exam Hours</th>
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<tr>
<td>04</td>
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<thead>
<tr>
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<td>52</td>
<td>100</td>
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**PART – A**

UNIT - 1
**DIGITAL IMAGE FUNDAMENTALS:** What is Digital Image Processing, fundamental Steps in Digital Image Processing, Components of an Image processing system, elements of Visual Perception.  
*6 Hours*

UNIT - 2
Image Sensing and Acquisition, Image Sampling and Quantization, Some Basic Relationships between Pixels, Linear and Nonlinear Operations.  
*6 Hours*
UNIT - 3
IMAGE TRANSFORMS: Two-dimensional orthogonal & unitary transforms, properties of unitary transforms, two dimensional discrete Fourier transform.  
7 Hours

UNIT - 4
Discrete cosine transform, sine transform, Hadamard transform, Haar transform, Slant transform, KL transform.  
7 Hours

PART – B

UNIT - 5
7 Hours

UNIT - 6
6 Hours

UNIT - 7
Model of image degradation/restoration process, noise models, Restoration in the Presence of Noise, Only-Spatial Filtering Periodic Noise Reduction by Frequency Domain Filtering, Linear Position-Invariant Degradations, inverse filtering, minimum mean square error (Weiner) Filtering.  
7 Hours

UNIT - 8
Color Fundamentals. Color Models, Pseudo color Image Processing., processing basics of full color image processing  
6 Hours

TEXT BOOK:

REFERENCE BOOKS:
PART – A

UNIT - 1
OVERVIEW OF WIRELESS PRINCIPLES: A brief history of wireless systems, Noncellular wireless applications, Shannon, Modulations & Alphabet Soup, Propagation. 3 Hours
PASSIVE RLC NETWORKS: Introduction, Parallel RLC Tank, Series RLC Networks, Other RLC networks, RLC Networks as impedance Transformers. 4 Hours

UNIT - 2
CHARACTERISTICS OF PASSIVE IC COMPONENTS: Introduction, Interconnect at radio frequencies: Skin effect, resistors, Capacitors, Inductors, Transformers, Interconnect options at high frequency. 6 Hours

UNIT - 3
A REVIEW OF MOS DEVICE PHYSICS: Introduction, A little history, FETs, MOSFET physics, The long – channels approximation, operation in weak inversion (sub threshold), MOS device physics in the short – channel regime, Other effects. 3 Hours
DISTRIBUTED SYSTEMS: Introduction, Link between lumped and distributed regimes driving-point impedance of iterated structures, Transmission lines in more detail, Behavior of Finite – length transmission lines, summary of transmission line equations, artificial lines. 4 Hours

UNIT - 4
PART – B

UNIT - 5
HIGH FREQUENCY AMPLIFIER DESIGN: Introduction, Zeros as bandwidth Enhancers, The shunt –series amplifier, Bandwidth Enhancement with fT Doublers, Tuned amplifiers, Neutralization and unilateralization, Cascaded amplifiers, AM – PM conversion. 7 Hours

UNIT - 6

UNIT - 7

UNIT - 8
Multiplier – based mixers, Sub sampling mixers, Diode ring mixers, RF power amplifiers, Introduction, general considerations, Class A, AB, B and C power amplifier, Class D amplifiers, Class E amplifiers Class F amplifiers, Modulation of power amplifiers, summary of PA characteristics, RF PA design examples, additional design considerations, Design summery. 7 Hours

TEXT BOOK:

REFERENCE BOOK:
PART – A

UNIT - 1
CONTINUOUS WAVELET TRANSFORM: Introduction, C-T wavelets, Definition of CWT, The CWT as a correlation. Constant Q-Factor Filtering Interpolation and time frequency resolution, the CWT as an operator, inverse CWT. 6 Hours

UNIT - 2
INTRODUCTION TO DISCRETE WAVELET TRANSFORM AND ORTHOGONAL WAVELET DECOMPOSITION: Introduction. Approximation of vectors in nested linear vector spaces, (i) example of approximating vectors in nested subspaces of a finite dimensional liner vector space, (ii) Example of approximating vectors in nested subspaces of an infinite dimensional linear vector space. Example MRA. (i) Bases for the approximations subspaces and Harr scaling function, (ii) Bases for detail subspaces and Haar wavelet. 7 Hours

UNIT - 3
MRA, ORTHO NORMAL WAVELETS AND THEIR RELATIONSHIP TO FILTER BANKS: Introduction, Formal definition of an MRA. Construction of a general orthonormal MRA, (i) scaling function and subspaces, (ii) Implication of dilation equation and orthogonality, a wavelet basis for MRA. (i) Two scale relations for (t), (ii) Basis for the detail subspace (iii) Direct sum decomposition, Digital filtering interpolation (i) Decomposition filters, (ii) reconstruction, the signal. 7 Hours

UNIT - 4
EXAMPLES OF WAVELETS: Examples of orthogonal basis generating wavelets, (i) Daubechies $D_4$ scaling function and wavelet. (ii) band limited wavelets, Interpreting orthonormal MRAs for Discrete time MRA, (iii) Basis functions for DTWT. 6 Hours
PART – B

UNIT – 5
ALTERNATIVE WAVELET REPRESENTATIONS: Introduction, Bi-orthogonal wavelet bases, Filtering relationship for bi-orthogonal filters, Examples of bi-orthogonal scaling functions and wavelets. 2-D wavelets.

6 Hours

UNIT – 6
Non - separable multidimensional wavelets, wavelet packets. Wavelets Transform and Data Compression: Introduction, transform coding, DTWT for image compression (i) Image compression using DTWT and run-length encoding.

7 Hours

UNIT – 7
(i) Embedded tree image coding (ii) compression with JPEG audio compression (iii) Audio masking, (iv) Wavelet based audio coding.

6 Hours

UNIT – 8

7 Hours

TEXT BOOK:

REFERENCE BOOKS:
MODELING AND SIMULATION OF DATA NETWORKS

Subject Code : 10EC766
IA Marks : 25
No. of Lecture Hrs/Week : 04
Exam Hours : 03
Total no. of Lecture Hrs. : 52
Exam Marks : 100

PART – A

UNIT – 1&2
DELAY MODELS IN DATA NETWORKS: Queuing Models, M/M/1, M/M/m, M/M/∞, M/M/m/m and other Markov System, M/G/1 System, Networks of Transmission Lines, Time Reversibility, Networks of Queues.
12 Hours

UNIT – 3&4
12 Hours

PART – B

UNIT – 5&6
14 Hours

UNIT – 7&8
FLOW CONTROL: Introduction, Window Flow Control, Rate Control Schemes, Overview of Flow Control in Practice, Rate Adjustment Algorithms.
14 Hours

REFERENCE BOOKS:
PART – A

UNIT - 1

UNIT - 2
Common Cellular System components, Common cellular network components, Hardware and software, views of cellular networks, 3G cellular systems components, Cellular component identification Call establishment.

UNIT - 3
Wireless network architecture and operation, Cellular concept Cell fundamentals, Capacity expansion techniques, Cellular backbone networks, Mobility management, Radio resources and power management Wireless network security.

UNIT - 4
GSM and TDMA techniques, GSM system overview, GSM Network and system Architecture, GSM channel concepts, GSM identifiers

PART – B

UNIT - 5
GSM system operation, Traffic cases, Call handoff, Roaming, GSM protocol architecture, TDMA systems.

UNIT - 6
CDMA technology, CDMA overview, CDMA channel concept CDMA operations.

UNIT - 7
Wireless Modulation techniques and Hardware, Characteristics of air interface, Path loss models, wireless coding techniques, Digital modulation
UNIT - 8
Introduction to wireless LAN 802.11X technologies, Evolution of Wireless LAN Introduction to 802.15X technologies in PAN Application and architecture Bluetooth Introduction to Broadband wireless MAN, 802.16X technologies.

TEXT BOOK:

REFERENCE BOOKS:

DIGITAL SWITCHING SYSTEMS

UNIT - 1
Developments of telecommunications, Network structure, Network services, terminology, Regulation, Standards. Introduction to telecommunications transmission, Power levels, Four wire circuits, Digital transmission, FDM, TDM, PDH and SDH, Transmission performance.
UNIT - 2
EVOLUTION OF SWITCHING SYSTEMS: Introduction, Message switching, Circuit switching, Functions of switching systems, Distribution systems, Basics of crossbar systems, Electronic switching, Digital switching systems. 6 Hours

DIGITAL SWITCHING SYSTEMS: Fundamentals: Purpose of analysis, Basic central office linkages, Outside plant versus inside plant, Switching system hierarchy, Evolution of digital switching systems, Stored program control switching systems, Digital switching system fundamentals, Building blocks of a digital switching system, Basic call processing. 7 Hours

UNIT - 3
TELECOMMUNICATIONS TRAFFIC: Introduction, Unit of traffic, Congestion, Traffic measurement, Mathematical model, lost call systems, Queuing systems. 6 Hours

UNIT - 4
SWITCHING SYSTEMS: Introduction, Single stage networks, Gradings, Link Systems, GOS of Linked systems. 6 Hours

PART – B

UNIT - 5
TIME DIVISION SWITCHING: Introduction, space and time switching, Time switching networks, Synchronisation. 6 Hours

UNIT - 6
SWITCHING SYSTEM SOFTWARE: Introduction, Scope, Basic software architecture, Operating systems, Database Management, Concept of generic program, Software architecture for level 1 control, Software architecture for level 2 control, Software architecture for level 3 control, Digital switching system software classification, Call models, Connect sequence, Software linkages during call, Call features, Feature flow diagram, Feature interaction. 7 Hours

UNIT - 7
maintainability, Embedded patcher concept, Growth of digital switching system central office, Generic program upgrade, A methodology for proper maintenance of digital switching system, Effect of firmware deployment on digital switching system, Firmware-software coupling, Switching system maintainability metrics, Upgrade process success rate, Number of patches applied per year, Diagnostic resolution rate, Reported critical and major faults corrected, A strategy improving software quality, Program for software process improvement, Software processes improvement, Software processes, Metrics, Defect analysis, Defect analysis.  

UNIT - 8

TEXT BOOKS:

REFERENCE BOOK:

ELECTIVE –IV (GROUP D)
DISTRIBUTED SYSTEM

<table>
<thead>
<tr>
<th>Subject Code</th>
<th>IA Marks</th>
</tr>
</thead>
<tbody>
<tr>
<td>10EC831</td>
<td>25</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>No. of Lecture Hrs/Week</th>
<th>Exam Hours</th>
</tr>
</thead>
<tbody>
<tr>
<td>04</td>
<td>03</td>
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</table>

<table>
<thead>
<tr>
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<tbody>
<tr>
<td>52</td>
<td>100</td>
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</table>

PART – A

UNIT - 1
CHARACTERIZATION OF DISTRIBUTED SYSTEMS: Introduction, Examples of distributed systems, Resource sharing and the web, Challenges.  

UNIT - 2
UNIT - 3
**INTERPROCESS COMMUNICATION:** Introduction, The API for the internet protocols, External data representation and marshalling, Clint-server communication, Group communication.  
*7 Hours*

UNIT - 4
**DISTRIBUTED OBJECTS AND REMOTE INVOCATION:** Introduction, Communication between distributed objects, Remote procedure call, Events and notifications.  
*6 Hours*

PART – B

UNIT - 5
**SECURITY:** Introduction, Overview of security technique cryptographic algorithms, Digital signature, Cryptography pragmatics.  
*7 Hours*

UNIT - 6
**TIME & GLOBAL STATES:** Introduction, Clocks, Events, Process states, Synchronizing physical clocks, Global states, Distributed debugging.  
*7 Hours*

UNIT - 7
**COORDINATION AND AGREEMENT:** Distributed mutual exclusion, Elections, Multicast communication.  
*6 Hours*

UNIT - 8
**CORBA CASE STUDY:** Introduction, CORBA RMI, CORBA Services.  
*6 Hours*

**TEXT BOOK:**

**REFERENCE BOOK:**
PART – A

UNIT - 1
Services, mechanisms and attacks, The OSI security architecture, A model for network security.  

6 Hours

UNIT - 2

7 Hours

UNIT - 3

6 Hours

UNIT - 4
Digital signatures, Authentication Protocols, Digital Signature Standard.  

7 Hours

PART – B

UNIT - 5
Web Security Consideration, Security socket layer (SSL) and Transport layer security, Secure Electronic Transaction.  

6 Hours

UNIT - 6
Intruders, Intrusion Detection, Password Management.  

6 Hours

UNIT - 7
MALICIOUS SOFTWARE: Viruses and Related Threats, Virus Countermeasures.  

7 Hours

UNIT - 8
Firewalls Design Principles, Trusted Systems.  

6 Hours
PART – A

UNIT - 1
INTRODUCTION TO OPTICAL NETWORKS: Telecommunication networks, First generation optical networks, Multiplexing techniques, Second generation optical networks, System and network evolution. Non linear effects SPM, CPM, four wave mixing, Solitons. 7 Hours

UNIT - 2
COMPONENTS: Couplers, isolators and Circulators, Multiplexes and filters Optical amplifiers. 6 Hours

UNIT - 3
Transmitters, detectors, Switches, Wavelength converters. 6 Hours

UNIT - 4
TRANSMISSION SYSTEM ENGINEERING: System model, Power penalty, Transmitter, receiver, optical amplifiers, Crosstalk, Dispersion, Overall design Consideration. 7 Hours

PART – B

UNIT - 5
FIRST GENERATION NETWORKS: SONET/SDH, Computer interconnects, Mans, Layered architecture for SONET and second generation networks. 6 Hours
UNIT - 6
WAVELENGTH ROUTING NETWORKS: Optical layer, Node design, Network design and operation, routing and wavelength assignment architectural variations.  

UNIT - 7
VIRTUAL TOPOLOGY DESIGN: Virtual topology design problem, Combines SONET/WDM network design, an ILP formulation, Regular virtual topologies, Control and management, Network management configuration management, Performance management, fault management.

UNIT - 8

TEXT BOOK:

REFERENCE BOOKS:

HIGH PERFORMANCE COMPUTER NETWORKS
Subject Code : 10EC834  IA Marks : 25
No. of Lecture Hrs/Week : 04  Exam Hours : 03
Total no. of Lecture Hrs. : 52  Exam Marks : 100

PART – A
UNIT - 1

UNIT - 2
NETWORK SERVICES AND LAYERED ARCHITECTURE: Applications, Traffic characterization and quality of services, Network

UNIT - 3

UNIT - 4
SONET, DWDM, FTH, DSL, Intelligent networks CATV.

PART – B

UNIT - 5
ATM: Main features of ATM, Addressing, signaling and Routing, ATM header structure, ATM AAL, Internetworking with ATM.

UNIT - 6

UNIT - 7
Control of networks, Objectives and methods of control, Circuit switched networks, Datagram Networks Network economics, Derived demand for network services, ISPs, subscriber demand model, Empirical model.

UNIT - 8
OPTICAL NETWORKS: WDM systems, Optical cross connects, Optical LANs, Optical paths and networks.

TEXT BOOK:

REFFRENCE BOOKS:
PART – A

UNIT - 1
INTRODUCTION: Communication model, Communication software, and communication protocol: Representation, Development methods, Protocol engineering process. NETWORK REFERENCE MODEL: Layered architecture, Network services and interfaces, protocol functions, OSI model, TCP/IP protocol suite, Application protocols. 7 Hours

UNIT - 2
PROTOCOL SPECIFICATION: Communication service specification, Protocol entity specification, Interface specifications, Interactions, Multimedia protocol specifications, Internet protocol specifications. 6 Hours

UNIT - 3
SPECIFICATION AND DESCRIPTION LANGUAGE (SDL): A protocol specification language: SDL. 6 Hours

UNIT - 4
Examples of SDL based protocol specifications, Other protocol specification languages. Protocol Verification And Validation, Protocol verification, Verification of a protocol using finite state machines. 7 Hours

PART – B

UNIT - 5
Protocol validation, Protocol design errors, and protocol validation approaches, SDL based protocol verification, SDL based protocol validation. 6 Hours

UNIT - 6
PROTOCOL CONFORMANCE TESTING: Conformance testing methodology and framework, Conformance test architectures, Test sequence generation methods, Distribute architecture by local methods, Conformance testing with TTCN, Conformance testing of RIP, Multimedia applications testing, SDL based tools for conformance testing. 7 Hours
UNIT - 7
PROTOCOL PERFORMANCE TESTING: SDL based performance testing of TCP, OSPF, Interoperability testing, SDL based interoperability testing of CSMA/CD and CSMA/CA protocol using bridge, Scalability testing.

7 Hours

UNIT - 8
PROTOCOL SYNTHESIS: Synthesis methods, interactive synthesis algorithms, automatic synthesis algorithm, automatic synthesis of SDL from MSC protocol re synthesis.

6 Hours

TEXT BOOK:

REFERENCES BOOKS:

ELECTIVE –V (GROUP E)
MULTIMEDIA COMMUNICATIONS

<table>
<thead>
<tr>
<th>Subject Code</th>
<th>IA Marks</th>
</tr>
</thead>
<tbody>
<tr>
<td>10EC841</td>
<td>25</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>No. of Lecture Hrs/Week</th>
<th>Exam Hours</th>
</tr>
</thead>
<tbody>
<tr>
<td>04</td>
<td>03</td>
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</tbody>
</table>

<table>
<thead>
<tr>
<th>Total no. of Lecture Hrs.</th>
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<td>100</td>
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PART – A

UNIT - 1
MULTIMEDIA COMMUNICATIONS: Introduction, multimedia information representation, multimedia networks, multimedia applications, media types, communication modes, network types, multipoint conferencing, network QoS application QoS.

6 Hours

UNIT - 2
MULTIMEDIA INFORMATION REPRESENTATION: Introduction, digital principles, text, images, audio, video.

7 Hours

UNIT - 3
TEXT AND IMAGE COMPRESSION: Introduction, compression principles, text compression, image compression.

6 Hours

107
UNIT - 4
7 Hours

PART – B

UNIT - 5
MULTIMEDIA INFORMATION NETWORKS: Introduction, LANs, Ethernet, Token ring, Bridges, FDDI High-speed LANs, LAN protocol.
6 Hours

UNIT - 6
7 Hours

UNIT - 7
BROADBAND ATM NETWORKS: Introduction, Cell format, Switch and Protocol Architecture ATM LANs.
6 Hours

UNIT - 8
TRANSPORT PROTOCOL: Introduction, TCP/IP, TCP, UDP, RTP and RTCP.
7 Hours

TEXT BOOK:

REFERENCE BOOKS:
PART – A

UNIT 1
Introduction to Real-Time Embedded Systems: Brief history of Real Time Systems, A brief history of Embedded Systems. 6 Hours

UNIT 2

UNIT 3
Processing: Preemptive Fixed-Priority Policy, Feasibility, Rate Monotonic least upper bound, Necessary and Sufficient feasibility, Deadline – Monotonic Policy, Dynamic priority policies. 6 Hours

UNIT 4
I/O Resources:
Memory:
Physical hierarchy, Capacity and allocation, Shared Memory, ECC Memory, Flash filesystems. 7 Hours

PART – B

UNIT 5
Multiresource Services:
Blocking, Deadlock and livestock, Critical sections to protect shared resources, priority inversion.

Soft Real-Time Services:
Missed Deadlines, QoS, Alternatives to rate monotonic policy, Mixed hard and soft real-time services. 7 Hours
UNIT 6  
**Embedded System Components:**  
Firmware components, RTOS system software mechanisms, Software application components.

**Debugging Components:**  
7 Hours

UNIT 7  
**Performance Tuning:**  
Basic concepts of drill-down tuning, hardware – supported profiling and tracing, Building performance monitoring into software, Path length, Efficiency, and Call frequency, Fundamental optimizations.  
6 Hours

UNIT 8  
**High availability and Reliability Design:**  
Reliability and Availability, Similarities and differences, Reliability, Reliable software, Available software, Design trade offs, Hierarchical applications for Fail-safe design.

Design of RTOS – PIC microcontroller. (Chap 13 of book Myke Predko)  
7 Hours

**REFERENCE BOOKS:**  

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**GSM**

<table>
<thead>
<tr>
<th>Subject Code</th>
<th>IA Marks</th>
</tr>
</thead>
<tbody>
<tr>
<td>10EC843</td>
<td>25</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>No. of Lecture Hrs/Week</th>
<th>Exam Hours</th>
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<tr>
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<td>100</td>
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**PART – A**

**GSM ARCHITECTURE AND INTERFACES:** Introduction, GSM frequency bands, GSM PLMN, Objectives of a GSM PLMN, GSM PLMN Services, GSM Subsystems, GSM Subsystems entities, GSM interfaces, The radio interface (MS to BSC), A_{bss} interface (BTS to BSC), A interface (BSC
UNIT - 2
RADIO LINK FEATURES IN GSM SYSTEMS: Introduction, Radio link measurements, Radio link features of GSM, Dynamic power control, Discontinuous transmission (DTX), SFH, Future techniques to reduce interface in GSM, Channel borrowing, Smart antenna. 7 Hours

UNIT - 3
GSM LOGICAL CHANNELS AND FRAME STRUCTURE: Introduction, GSM logical channels, Allowed logical channel combinations, TCH multi frame for TCH/H, CCH multi frame, GSM frame structure, GSM bursts, Normal burst, Synchronization burst, Frequency correction channel burst, Access burst, Data encryption in GSM, Mobility management, Location registration, Mobile identification. 7 Hours

UNIT - 4
SPEECH CODING IN GSM: Introduction, Speech coding methods, Speech code attributes, Transmission bit rate, Delay, Complexity, Quality, LPAS, ITU-T standards, Bit rate, Waveform coding, Time domain waveform coding, Frequency domain waveform coding, Vocoder, Full-rate vocoder, Half-rate vocoder. MESSAGES, SERVICES, AND CALL FLOWS IN GSM: Introduction, GSM PLMN services. 7 Hours

PART – B

UNIT - 5
GSM messages, MS-BS interface, BS to MSC messages on the A interface, MSC to VLR and HLR, GSM call setup by an MS, Mobile-Terminated call, Call release, Handover. Data services, Introduction, Data interworking, GSM data services, Interconnection for switched data, Group 3 fax, Packet data on the signaling channel, User-to-user signaling, SMS, GSM GPRS. 6 Hours

UNIT - 6
PRIVACY AND SECURITY IN GSM: Introduction, Wireless security requirements, Privacy of communications, Authentication requirements, System lifetime requirements, Physical requirements, SIM cards, Security algorithms for GSM, Token-based authentication, Token-based registration, Token-based challenge. 6 Hours

UNIT - 7
PLANNING AND DESIGN OF A GSM WIRELESS NETWORK: Introduction, Tele traffic models, Call model, Topology model, Mobility in
cellular / PCS networks, Application of a fluid flow model, Planning of a wireless network, Radio design for a cellular / PCS network, Radio link design, Coverage planning, Design of a wireless system, Service requirements, Constraints for hardware implementation, Propagation path loss, System requirements, Spectral efficiency of a wireless system, Receiver sensitivity and link budget, Selection of modulation scheme, Design of TDMA frame, Relationship between delay spread and symbol rate, Design example for a GSM system.

7 Hours

UNIT - 8
MANAGEMENT OF GSM NETWORKS: Introduction, Traditional approaches to NM, TMN, TMN layers, TMN nodes, TMN interface, TMN management services, Management requirements for wireless networks, Management of radio resources, Personal mobility management, Terminal mobility, Service mobility management, Platform-centered management, SNMP, OSI systems management, NM interface and functionality, NMS functionality, OMC functionality, Management of GSM network, TMN applications, GSM information model, GSM containment tree, Future work items.

7 Hours

TEXT BOOK:

REFERENCE BOOKS:

ADHOC WIRELESS NETWORKS

<table>
<thead>
<tr>
<th>Subject Code</th>
<th>IA Marks</th>
</tr>
</thead>
<tbody>
<tr>
<td>10EC844</td>
<td>25</td>
</tr>
<tr>
<td>No. of Lecture Hrs/Week</td>
<td>Exam Hours</td>
</tr>
<tr>
<td>04</td>
<td>03</td>
</tr>
<tr>
<td>Total no. of Lecture Hrs.</td>
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<td>52</td>
<td>100</td>
</tr>
</tbody>
</table>

PART – A

UNIT - 1
AD HOC NETWORKS: Introduction, Issues in Ad hoc wireless networks, Ad hoc wireless internet. 6 Hours

112
UNIT - 2
MAC PROTOCOLS FOR AD HOC WIRELESS NETWORKS:
Introduction, Issues in designing a MAC protocol for Ad hoc wireless Networks, Design goals of a MAC protocol for Ad hoc wireless Networks, Classification of MAC protocols. 7 Hours

UNIT - 3
Contention-based MAC protocols with scheduling mechanism, MAC protocols that use directional antennas, Other MAC protocols. 6 Hours

UNIT - 4
ROUTING PROTOCOLS FOR AD HOC WIRELESS NETWORKS:
Introduction, Issues in designing a routing protocol for Ad hoc wireless Networks, Classification of routing protocols, Table drive routing protocol, On-demand routing protocol. 7 Hours

PART – B

UNIT - 5
Hybrid routing protocol, Routing protocols with effective flooding mechanisms, Hierarchical routing protocols, Power aware routing protocols. 6 Hours

UNIT - 6
TRANSPORT LAYER PROTOCOLS FOR AD HOC WIRELESS NETWORKS: Introduction, Issues in designing a transport layer protocol for Ad hoc wireless Networks, Design goals of a transport layer protocol for Ad hoc wireless Networks. 7 Hours

UNIT - 7
SECURITY: Security in wireless Ad hoc wireless Networks, Network security requirements, Issues & challenges in security provisioning. 6 Hours

UNIT - 8
QUALITY OF SERVICE IN AD HOC WIRELESS NETWORKS:
Introduction, Issues and challenges in providing QoS in Ad hoc wireless Networks, Classification of QoS solutions. 7 Hours

TEXT BOOK:
REFERENCE BOOKS:
1. “Ad hoc wireless Networks”, Ozan K. Tonguz and Gianguigi Ferrari, Wiley

OPTICAL COMPUTING

<table>
<thead>
<tr>
<th>Subject Code</th>
<th>IA Marks</th>
</tr>
</thead>
<tbody>
<tr>
<td>10EC845</td>
<td>25</td>
</tr>
<tr>
<td>No. of Lecture Hrs/Week</td>
<td>Exam Hours</td>
</tr>
<tr>
<td>04</td>
<td>03</td>
</tr>
<tr>
<td>Total no. of Lecture Hrs.</td>
<td>Exam Marks</td>
</tr>
<tr>
<td>52</td>
<td>100</td>
</tr>
</tbody>
</table>

PART – A

UNIT - 1
MATHEMATICAL AND DIGITAL IMAGE FUNDAMENTALS:
Introduction, Fourier Transform, discrete Fourier transform, basic diffraction theory, Fourier transform property of lens, sampling and quantization, image enhancement, image restoration.  

UNIT - 2

UNIT - 3
ANALOG OPTICAL ARITHMETIC: Introduction, Halftone processing, nonlinear optical processing, Arithmetic operations.

UNIT - 4

PART – B

UNIT - 5
UNIT - 6
SHADOW-CASTING AND SYMBOLIC SUBSTITUTION: Introduction, Shadow casting system and design algorithm, POSC logic operations, POSC multiprocessor, Parallel ALU using POSC, Sequential ALU using POSC, POSC image processing, Symbolic substitutions, Optical implementation of symbolic substitution, Limitations and challenges. 7 Hours

UNIT - 7
OPTICAL MATRIX PROCESSING: Introduction, Multiplication, Multiplication using convolution, Matrix operations, Cellular logic architecture, Programmable logic array. 6 Hours

UNIT - 8
ARTIFICIAL INTELLIGENT COMPUTATIONS: Introduction, Neural networks, Associative memory, Optical implementations, Interconnections, Artificial Intelligence. 7 Hours

TEXT BOOK:

REFERENCE BOOKS:

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